Antimony Semimetal Contact with Enhanced Thermal Stability for High Performance 2D Electronics

Ang-Sheng Chou[1*], Tong Wu[2], Chao-Ching Cheng[1], Shun-Siang Zhan[3], I-Chih Ni[3], Shih-Yun Wang[4], Yu-Chen Chang[4], San-Lin Liew[6], Edward Chen[1], Wen-Hao Chang[4], Chih-I Wu[3], Jin Cai[5], H.-S. Philip Wong[1] and Han Wang[2*]
[1]Corporate Research, TSMC, Hsinchu, Taiwan; [2]Corporate Research, TSMC, San Jose, CA, USA; [3]Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan; [4]Department of Electrophysics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan; [5]Pathfinding, TSMC, Hsinchu, Taiwan [6]Quality & Reliability, TSMC, Hsinchu, Taiwan
*email: hanwang@tsmc.com, aschoua@tsmc.com

Abstract – Antimony (Sb) semimetal was studied as a novel contact approach for enabling two-dimensional (2D) material towards advanced electronic device applications. With this approach, an ohmic contact of close to zero Schottky barrier height and contact resistance value of 0.66 kΩ.μm is obtained between Sb and monolayer (1L) molybdenum disulfide (MoS_2). Short-channel Sb-contacted MoS_2 field-effect transistors (FET) demonstrated remarkable on-state current above 600 μA/μm and 1000 μA/μm at V_{DS} = 1 V and 2 V, respectively. Comparing to our previous study of tin (Sn) [1] and bismuth (Bi) semimetal contacts [2], Sb contact offers substantially improved thermal stability with a melting point of 630.6 °C as compared to 271.5 °C for Bi and 231.9 °C for Sn semimetals. The comparative electrical characterization of MoS_2 FETs with Sb and Bi contacts after progressive thermal treatments demonstrates fully operational Sb-contacted devices after annealing at 400 °C in contrast to 300 °C for Bi-contacted devices, indicating the advantage of Sb towards reaching the thermal budget for back-end-of-the-line (BEOL) compatibility, and hence alleviating the major shortcoming of previously studied Bi and Sn semimetals in terms of their thermal stability issue. The study demonstrates the clear benefits of Sb as a novel semimetal contact option with applications in high performance 2D material device towards beyond-silicon electronics technology.

I. INTRODUCTION

Semimetals offer unique advantages in suppressing metal-induced gap states (MIGS) and in inducing states degeneracy at the contact interface due to the absence of bandgap and minimal density of states at their Fermi level (Fig. 1), and hence are promising ultralow resistance contact solutions for 2D materials towards advanced electronics application. However, previously studied semimetals such as Sn [1] and Bi [2] may suffer from significant thermal stability issues and process compatibility due to their very low melting points, both below 300 °C. In this work, we report the first study of Sb as a novel semimetal contact solution with improved thermal stability for 2D materials. The key contribution of this work is four-folds: (i) Sb semimetal is studied as the contact metal for 2D materials for the first time, demonstrating one of the lowest contact resistance among previously reported approaches for MoS_2 only second to Bi; (ii) short-channel (L_{CH}=50 nm) monolayer MoS_2 FET with Sb contact demonstrates high on-state current (I_{ON}) exceeding 600 μA/μm at V_{DS} = 1 V; (iii) Thermal treatment study of Sb and Bi semimetals in configurations as both pure metal line and as device contact indicate substantial thermal stability advantage of Sb contact above 300 °C as compared to Bi contact, with Sb-contacted 1L MoS_2 FET maintaining 80% and 64% of the pristine sample performance after annealing at 300 °C and 400 °C, respectively, and record performance for 1L MoS_2 FETs among those that can satisfy BEOL thermal compatibility requirements. (iv) multi-scale simulation and modeling study revealed promising prospects of Sb-Bi alloy contact strategy towards reaching even lower contact barrier while still maintaining high thermal integrity.

II. APPROACH

Sb semimetal contacts on monolayer MoS_2 are experimentally and theoretically studied at both the material and device levels. Their thermal reliability is evaluated and compared with respect to Bi contact for 1L MoS_2 FETs in terms of contact resistance and on-state current. Theoretical study (Fig. 2, 3) is carried out to understand the interface barrier and device characteristics. In addition, we projected the properties of Bi-Sb semimetal alloy towards balanced electrical performance and thermal stability.

A. Devices Fabrication and Charecterization

All the MoS_2 FETs reported in this work use 1L MoS_2 grown by chemical vapor deposition (CVD) method. As described in Fig. 5, CVD-1L-MoS_2 was transferred onto commercial 100 nm SiN_x/Si substrate. Helium-ion-beam lithography was used to pattern the S/D contact electrodes, which were deposited with 20 nm semimetal (Bi or Sb) capped by 15 nm Au using e-beam evaporation and lift-off. The encapsulation process is to use PMMA as a protective layer and hard baking at 200 ℃ for 30 minutes in glove box with N_2 environment. The device is hysteresis-free and maintain the original electrical properties after protection coating. The I–V characteristics of devices were measured in Lakeshore probe station and Agilent 4156C parameter analyzer at room temperature in vacuum. Thermal annealing is progressively performed at 200 °C, 300 °C and 400 °C. Raman spectroscopy, atomic force microscopy (AFM), and transmission electron microscopy (TEM) analysis were used to characterize the material and contact interface properties. Energy-dispersive X-ray spectroscopy (EDS) mapping was used to reveal elements composition at the interface region.

B. Simulation and Modeling

To atomistically simulate the interface characteristics between semimetals (Sb, Bi) and MoS_2, the density-functional theory (DFT) is implemented with Perdew–Burke–Ernzerhof (PBE) exchange-correlation function, the projector augmented wave method (PAW) and generalized gradient approximation (GGA) method in Vienna ab-initio simulation package (VASP). The structure is optimized with a tolerance of 10 μeV. The Brillouin-zone was sampled by the Monkhorst-Pack scheme with a grid ensuring $k \times \vec{a} > 40$Å. The cutoff energy is set to 520 eV. The energy grid is 50 points/eV.

III. RESULTS

A. Contact Interface Properties

Fig. 2 compares the electron density distribution at the Sb-MoS_2 and Bi-MoS_2 interfaces. The Sb-MoS_2 interface shows a higher electron density closer to the semimetal side than that at the Bi-

2021 IEEE International Electron Devices Meeting (IEDM) | 978-1-6654-2572-8/21/$31.00 ©2021 IEEE | DOI: 10.1109/IEDM19574.2021.9720608

Authorized licensed use limited to: The University of Hong Kong Libraries. Downloaded on May 10,2024 at 02:52:36 UTC from IEEE Xplore. Restrictions apply.

MoS_2 interface. The corresponding band structure at the contact region is also simulated (Fig. 3). The Sb-MoS_2 heterostructure demonstrates lower density of states at the Fermi level region, indicating that it has less MIGS compared to the Bi-MoS_2 structure. Sb has a slightly higher work function than Bi. It can also be more difficult to achieve state degeneracy at Sb-MoS_2 interface as compared to the Bi-MoS_2 case due to their different interface dipole direction, as verified by Ultraviolet photoemission spectroscopy measurement (UPS, Fig. 4).

B. Device characteristics and thermal reliability:

Fig. 6-7 compare the transfer (I_D-V_{GS}) and output (I_D-V_{DS}) characteristics of pristine (without intentional annealing) short-channel MoS_2 nFETs with Bi and Sb contacts. Bi- and Sb-contacted MoS_2 FETs (L_{CH} = 100 nm) achieves I_{ON} of ~544 and ~495 μA/μm at V_{DS} = 1 V, respectively, both with excellent I_{ON}/I_{OFF} ratio of ~10^7. Linear I_D-V_{DS} characteristics at low bias are indicative of ohmic contact behavior and low Schottky barrier heights in both devices. The corresponding SEM and TEM images of the Sb-contacted MoS_2 device are presented in Fig. 8 where the L_{CH} defined by the minimum space of S/D contacts is ~100 nm. In Fig. 9, the thickness of MoS_2 grown on sapphire and then transferred to SiN/Si substrate as measured by AFM is ~1 nm. The Raman spectrum in Fig 9 shows characteristic peaks of 1L MoS_2. A redshift is observed for both the out-of-plane A1′ and in-plane E′ modes after thermal annealing, implying possible thermally induced strain effect on MoS_2 channel [3]. Fig. 10 shows the TEM image and corresponding EDS mapping of the Sb-MoS_2 contact region after the sample was annealed at 300 ⁰C. Good adhesion between Sb semimetal and 1L-MoS_2 is preserved after the thermal processing without any observable damage. Fig. 11 and 12 compare the electrical characteristics of the Sb-contacted MoS_2 device before and after 300 ℃ annealing. The device still maintains a high I_{ON} of ~375 μA/μm (V_{DS} = 1 V) after annealing at 300 ℃. Further analysis shows that the performance degradation mainly results from increased contact resistance while the mobility of MoS_2 extracted using the Y-function method remains similar after annealing (Fig. 13). Hence, one possible cause for the performance degradation after annealing can be the thermally induced strain effect at the Sb-MoS_2 interface that degrades the interface quality. Figs. 14-15 shows the electrical characteristics of a shorter channel device (L_{CH} = 50 nm) that gives even higher I_{ON} ~ 600 μA/μm at V_{DS}= 1V and nearly zero drain-induced barrier lowering (DIBL).

Fig. 16 compares the effect of total 40 minutes thermal annealing at progressively higher temperatures on the contact resistance and mobility extracted from both the Bi- and Sb-contacted MoS_2 FETs. It is observed that Bi contact degraded severely after annealing at 300 ℃ due to its low melting point. The device did not fail completely possibly because the encapsulation layer could restrict the diffusion of Bi, and Au capping may also serve as a partial contact. Sb contact is functional after annealing at significantly higher temperature (400 ℃), showing a smaller degree of performance degradation. Fig. 17 compares the on-state current of MoS_2 FETs with Bi and Sb contacts after progressive thermal annealing at 200 ℃, 300 ℃ and 400 ℃. The Sb-contacted MoS_2 FET can retain 80% and 64% performance after annealing at 300 ℃ and 400 ℃, respectively. In contrast, the performance of the Bi-contacted device decayed significantly after annealing at 300 ℃ and failed completely at 400 ℃. To further evaluate the thermal stability of pure Bi and Sb semimetals themselves, 100 μm line test structures made from only the semimetals (inset of Fig. 18) without MoS_2 were fabricated and tested. The Bi line failed completely when the annealing temperature rises above its melting point at 300 ℃. Meanwhile, Sb line survived well after annealing at 400 ℃ (Figs. 18-19). Note that this line test is a more stringent test on the semimetal thermal stability than the FET test since the conductivity of semimetal line can fail as long as failure occurs at any weak link along the 100 μm length of the line structure. Table I benchmarks the work function, melting point, lattice constant, and the best contact resistance achieved on 1L MoS_2 (at carrier density, $n_{2D} > 10^{13}$ cm^{-2}) for different semimetals [1-2, 4], demonstrating the advantage of Sb semimetal in reaching the best balance between the thermal stability and the contact resistance performance.

C. DFT simulation and Bi-Sb Alloy Contact Properties

Experimental results show that Bi semimetal may provide lower contact resistance than Sb, but with worse thermal stability. Hence, more optimal balance between thermal stability and contact resistance may be achieved through creating alloy between Bi and Sb semimetals. DFT simulation is carried out to predict the properties of the Bi-Sb alloy and their interface characteristics with respect to 1L MoS_2 [5]. Specifically, barrier height at the alloy-1L-MoS_2 contact is plotted in Fig. 20 together with the melting point of Bi-Sb alloy as a function of the alloying ratio. The barrier height of the alloy-MoS_2 contact increases with increasing Sb ratio, which can exponentially impact the tunneling current according to the WKB approximation. On the other hand, the melting point of the alloy also increases with the Sb ratio [6-7]. For BEOL compatibility, a melting point of at least 400 ℃ is essential, which requires Sb ratio greater than 20%. In addition, the alloy is predicted to behave as semiconductor/topological insulator with a small bandgap for Sb ratio 4%-40%, which is not desirable as a contact material. Hence, there is a preferred design space with Sb ratio from 40% to 100% as highlighted by the green box in Fig. 20. A good trade-off among the barrier height, alloy conductivity and alloy melting point can be achieved in this region. For example, $Bi_{0.5}Sb_{0.5}$ can offer a lower barrier height (0.10 eV) than pure Sb, while maintaining good conductivity and melting point of 540 ℃.

IV. CONCLUSION

An exploratory study of a novel contact approach for 2D materials using Sb semimetal has been carried out, covering fundamental material and interface characterization, device demonstration, as well as comparative thermal stability study and benchmarking. Low contact resistance and high on-state current are both demonstrated for short-channel MoS_2 FET down to 50 nm channel length. Thermal treatment test shows Sb-contacted MoS_2 FETs operational after 400 °C thermal annealing. These devices demonstrate contact resistance and on-state current that can sustain high temperature treatment above 300 °C, and are hence a promising contact option for MoS_2 FETs towards achieving thermal compatible with BEOL process, which outperforms the previously reported Sn and Bi semimetal contacts. With multi-scale device simulations, this work also elucidates the Sb/MoS_2 contact interface characteristics and the prospective of engineering Sb-Bi alloy towards further improved contact solution that can balance both thermal stability and low contact resistance for 2D material electronics technology.

ACKNOWLEDGMENT: This work was supported by the Ministry of Science and Technology (Grant No. MOST-109-2622-8-002-003; Grant No. MOST 110-2119-M-A49-001-MBK).

REFERENCES: [1] A.-S. C. *et al*., *IEEE Electron Device Letters*, 42, 2, pp. 272-275 (2021). [2] P.-C. S. *et al., Nature,* 593, 211–217 (2021). [3] L. Zhang *et al., Nano Lett.*, 19, 4745−4751 (2019). [4] S.-S. C. *et al., Adv. Mater.*, 31, 1804422 (2019). [5] B. Ouyang *et al., npj 2D Mater Appl*, 2, 13 (2018). [6] https://www.engineeringtoolbox.com/melting-points-mixtures-metals-d_1269.html [7] D. Hsieh *et al., Nature,* 452, 970–974 (2008).

Authorized licensed use limited to: The University of Hong Kong Libraries. Downloaded on May 10,2024 at 02:52:36 UTC from IEEE Xplore. Restrictions apply.

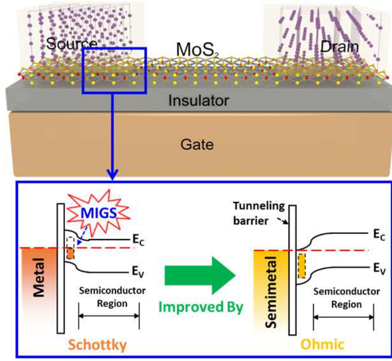

Fig. 1. Schematic of 1L MoS_2 channel FET with semimetal contact. Lower panel indicates the advantages of semimetal contact for reducing MIGS and achieving states degeneracy at contact interface.

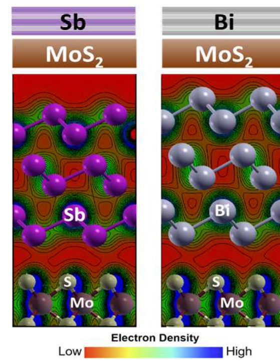

Fig. 2. DFT simulated charge densities mapping at the Sb-MoS_2 (left) and Bi- MoS_2 (right) interfaces.

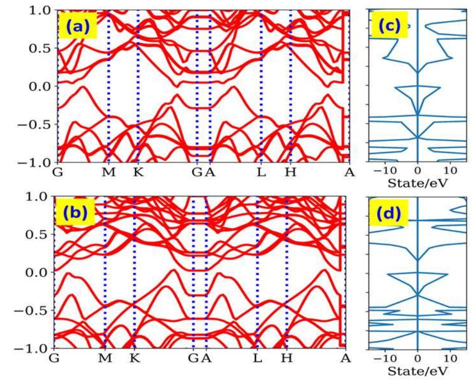

Fig. 3. The simulated band structure along the high symmetry k direction of the (a) Sb-MoS_2 (b) Bi-MoS_2 heterostructure, and (c, d) are the corresponding density of states.

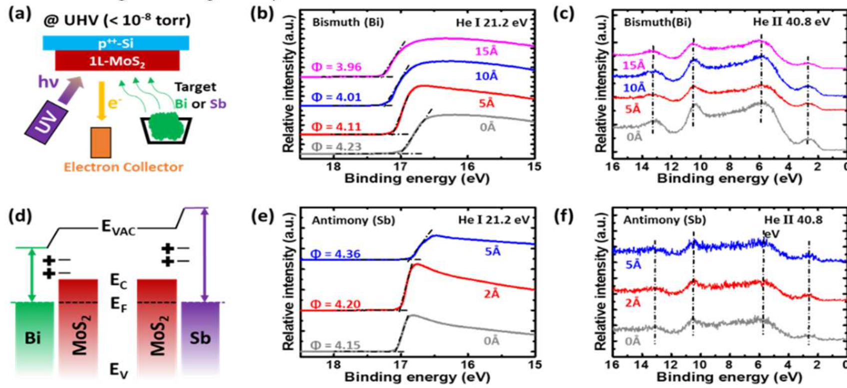

Fig. 4. (a) Schematic of the experimental setup for stepwise semimetal deposition in UHV with in-situ UPS measurement. UPS analyzed at (b, e) onset of secondary electron emission, and (c, f) the valence band of semimetal/MoS_2 interface. (d) Schematic illustration showing band alignment at the semimetal/MoS_2 interface.

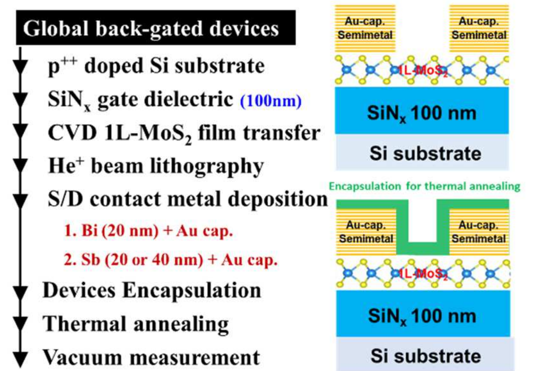

Fig. 5. Key process steps of 1L MoS_2 device fabrication with semimetal contacts and thermal annealing tests.

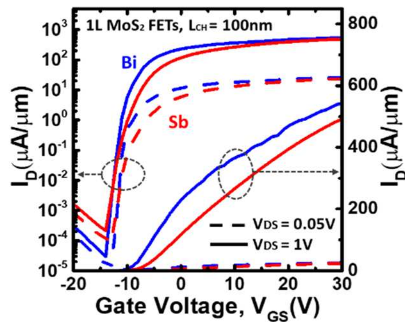

Fig. 6. Log/linear plots of the transfer characteristics (I_D-V_{GS}) of CVD 1L-MoS_2 FETs with Bi and Sb S/D contacts. Both devices have the same L_{CH} of ~100 nm and 100 nm SiN_x gate dielectric.

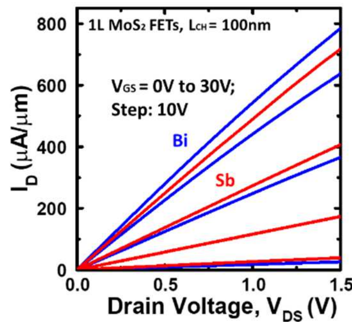

Fig. 7. Output characteristics (I_D-V_{DS}) of CVD 1L-MoS_2 FETs with Bi and Sb S/D contacts. Current linearity at low bias indicates low Schottky barrier (Ohmic-like) in both devices.

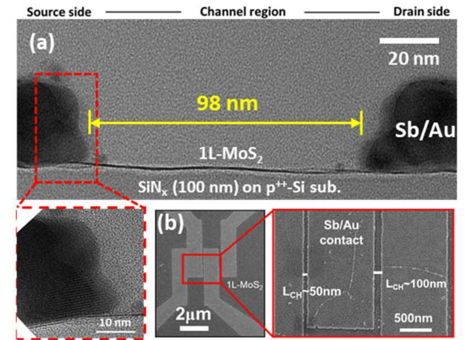

Fig. 8. (a) High resolution cross-sectional TEM images of Sb/Au contact on 1L MoS_2 with excellent adhesion, and (b) SEM images of short channel back-gated devices, patterned by He^+ beam lithography.

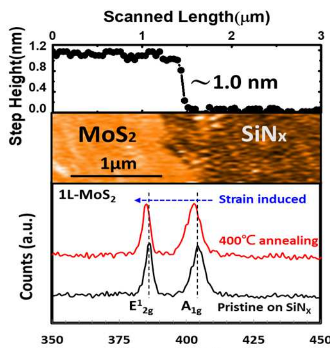

Fig. 9. Characterizations of a CVD 1L MoS_2 film. (a) AFM and (b) Raman spectrum analysis before and after annealing.

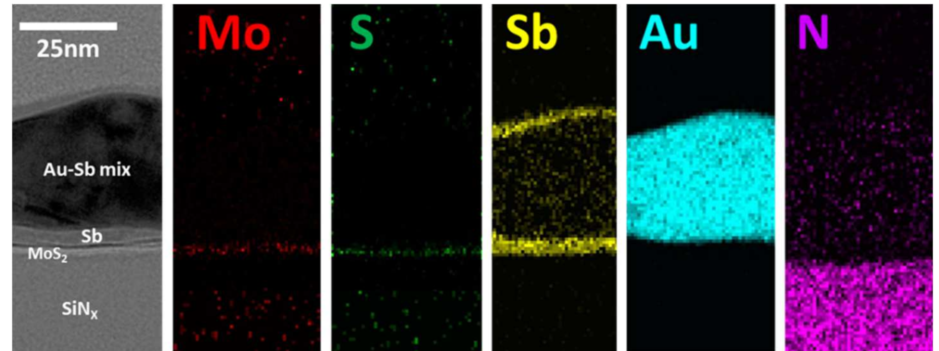

Fig. 10. (a) High resolution cross-sectional TEM images of Sb/Au contact on CVD 1L-MoS_2 after 300 °C thermal annealing, and EDS mapping of Mo, S, Sb, Au, and N elemental distribution. Note: the mixing of the Au-Sb metals in the upper part of the contact is not due to the annealing process, but occurred during the deposition.

Authorized licensed use limited to: The University of Hong Kong Libraries. Downloaded on May 10,2024 at 02:52:36 UTC from IEEE Xplore. Restrictions apply.

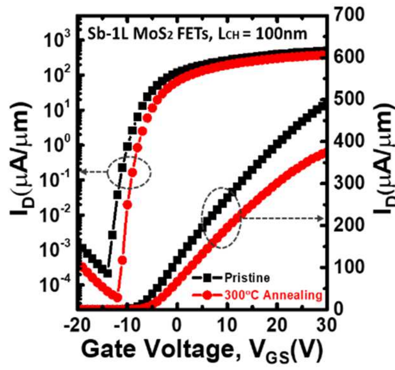

Fig. 11. Transfer characteristics (I_D-V_{GS}) of the Sb-contacted MoS_2 FET before and after annealing at 300ºC. V_{DS}=1 V.

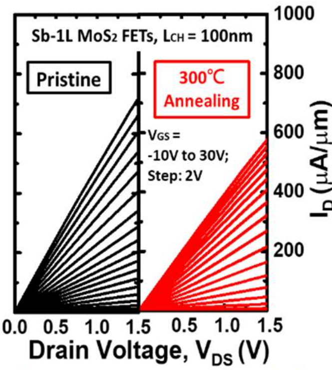

Fig. 12. Output characteristics (I_D-V_{DS}) corresponding to the same device in Fig. 11 before and after annealing at 300ºC.

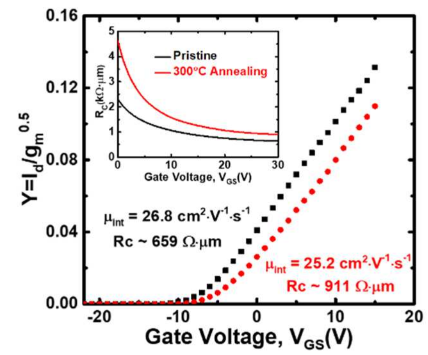

Fig. 13. Extraction of intrinsic mobility and contact resistance by Y-function method. The mobility remained similar and contact resistance increased after annealing.

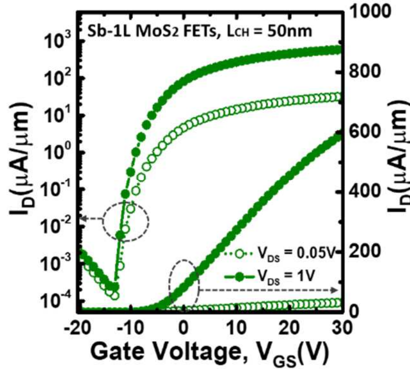

Fig. 14. Transfer characteristics (I_D-V_{GS}) of a further scaled Sb-contacted MoS_2 FET with L_{CH} = 50 nm, showing minimal DIBL.

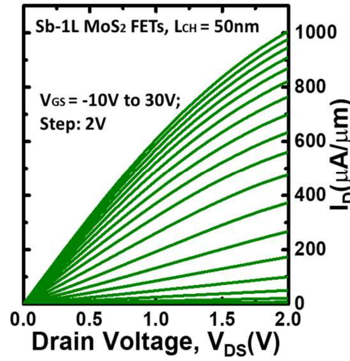

Fig. 15. Output characteristic (I_D-V_{DS}) of the same Sb-contacted MoS_2 FET as in Fig. 14 with L_{CH} = 50 nm.

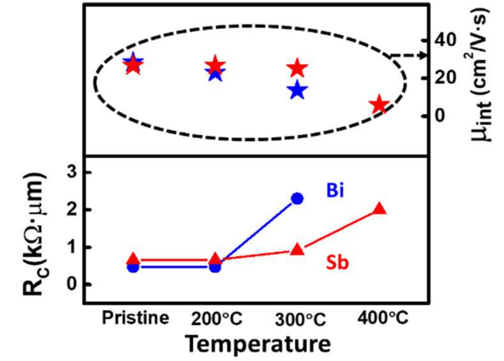

Fig. 16. Changes in the contact resistance and intrinsic mobility after progressive annealing. Sb-contacts clearly demonstrates enhanced thermal stability than Bi-contacts.

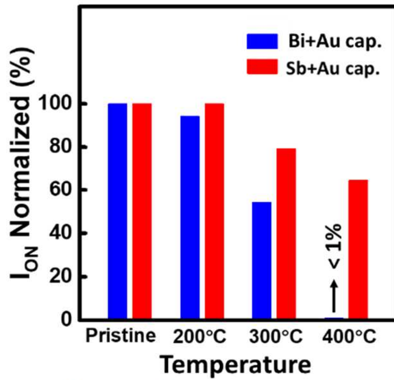

Fig. 17. Comparison of on-state current in MoS_2 FETs with Bi and Sb contacts after progressive thermal annealing. Sb-contacted MoS_2 FET can retain 80% and 64% performance after annealing at 300°C and 400°C, respectively. In contrast, Bi-contacted MoS_2 FET completely fails after annealing at 400°C.

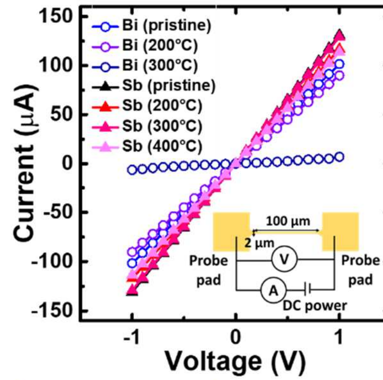

Fig. 18. Electrical characterization of the semimetal lines after annealing at different temperatures. Inset: schematic of the 40 nm thick interconnect line structure.

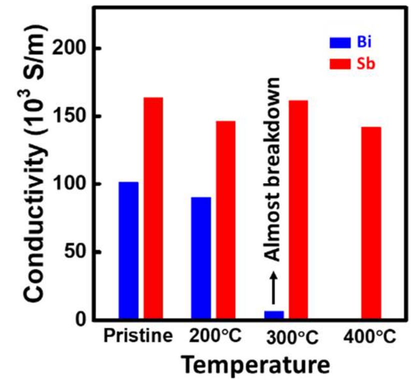

Fig. 19. Bi and Sb semimetal line conductivity with progressive annealing. Sb maintains similar conductivity after annealing at 400 ºC. In contrast, Bi was melted and appear clustered after annealing at 300°C.

	Tin (Sn)	Bismuth (Bi)	Antimony (Sb)	Arsenic (As)	Graphene
Melting point (℃)	231.9	271.5	630.6	817.0	> 3600
Work function (eV)	4.42	4.1	4.4	4.7	4.5
Lattice constant (Å)	a: 5.83 b: 5.83 c: 3.18	a: 6.67 b: 6.12 C: 3.30	a: 4.31 b: 4.31 c: 11.27	a: 3.76 b: 3.76 c: 10.55	a: 2.46
Contact resistance on 1L-MoS_2 (kΩ·μm)	0.84 [1]	0.12 [2]	0.66 (This work)	N/A	115 [4]

Table I. Benchmark of different semimetals, including melting point, work function, lattice constant and their contact resistances on monolayer MoS_2.

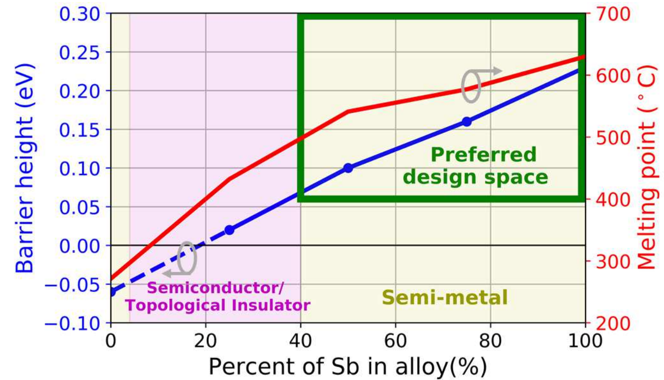

Fig. 20. Simulated barrier height of the Bi-Sb alloy with respect to monolayer MoS_2, together with their melting point. The blue line is the barrier height at the alloy-MoS_2 interface, with Fermi level of MoS_2 at 4.4 eV. The red line is the melting temperature of Bi-Sb alloy. When the alloy ratio of Sb is at 4%-40%, the alloy is a semiconductor/topological insulator with band gap <0.02 eV. While for the other ratio range of Sb (0%-4% and 40%-100%), the alloy is a semi-metal. Negative value of barrier height indicates state degeneracy.

Authorized licensed use limited to: The University of Hong Kong Libraries. Downloaded on May 10,2024 at 02:52:36 UTC from IEEE Xplore. Restrictions apply.