High-Performance Monolayer WSe_2 p/n FETs via Antimony-Platinum Modulated Contact Technology towards 2D CMOS Electronics

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Abstract – Low resistance contact technology for 2D semiconductors is a key bottleneck for the practical application of 2D channel materials at advanced logic nodes. This work presents a novel Sb-Pt modulated contact technology which can alleviate the Fermi-level pinning effect and mediate the band alignment at the metal-2D semiconductor interface, leading to exceptional ohmic contacts for both p-type and n-type WSe_2 FETs (p/n FET). WSe_2 FETs with different Sb/Pt contact compositions, in combination with new oxide-based encapsulation/doping technologies, exhibits record low pFET contact resistance of 0.75 kΩ·μm among all reported monolayer (1L) 2D pFETs. The nFET contact resistance of 1.8 kΩ·μm is also the lowest among 1L WSe_2 nFETs. Both 1L WSe_2 pFET and nFET demonstrated remarkable on-state p/n current ~150 μA/μm at $|V_D|$=1 V, indicating the potential of WSe_2 for CMOS applications. A new version of the semi-automated dry transfer process for chemical vapor deposition (CVD) WSe_2 was also developed utilizing a novel Bi/PMMA/TRT support stack, offering low defect wrinkle-free WSe_2 transfer at wafer-scale.

I. Introduction

2D semiconducting transition metal dichalcogenides (TMD) are promising as atomically thin channel materials for future post-silicon CMOS transistor technology at the ultimate scale [1]. However, achieving low resistance contact for 2D semiconductor p/n FETs remains a crucial challenge towards such technology insertion at advanced technology nodes. Recent development of semimetallic contacts (e.g. Bi [2] and Sb [3]) as well as low-melting-point metal contacts (e.g. Sn and In) [4] have demonstrated reduction in contact resistance (R_C) and good performance for nFETs. However, the performances of pFETs made with TMDs are still one to two orders of magnitude lower, because these proposed contact metals for TMD nFETs have improper band alignments for hole conductions, leading to high Schottky barrier (SB), high R_C and poor current-delivery capability. WSe_2 has been proposed as a promising TMD with ambipolar conduction characteristics, and the recent development of reliable and scalable synthesize and transfer technologies for TMDs, including monolayer WSe_2, have paved the way towards practical applications. In this work, we develop a contact modulation technology based on Sb-Pt stacked deposition, which can relieve the Fermi-level pinning effect and offers work function tuning with different chemical compositions. This technology, in combination with proper channel capping layers, gives rise to low R_C for both electron and hole conductions towards enabling high performance CMOS technologies based on monolayer CVD WSe_2. *The key contributions of this work are four-folds:* (i) a new version of semi-automated wafer-scale low defect transfer process based on Bi interfacial layers and PMMA/TRT support layer is demonstrated; (ii) Sb semimetal is mixed with high work function metal Pt as a modulated contact technology for monolayer WSe_2, which enables low R_C for both pFETs and nFETs; (iii) new MoO_x and $SiON_x$ channel capping/doping technologies are developed for 1L WSe_2 pFET and nFET, respectively, to further boost the device performance. (iv) The proposed device technologies have led to hysteresis-free I-V characteristics, low SB heights close to thermal voltage at room temperature, record low R_C value down to 0.75 kΩ·μm and 1.8 kΩ·μm and high on-state current of 151 μA/μm and 147 μA/μm, for 1L WSe_2 pFETs and nFETs, respectively.

II. Approach

A. Bi-Assisted Dry Transfer of Wafer-Scale WSe_2

Throughout this study, 1L WSe_2 was used as the channel material, grown by CVD. CVD-1L-WSe_2 was transferred onto 100 nm SiN_x/Si substrates by a new version of the bismuth (Bi)-assisted dry transfer technology that we previously developed in-house [5], with novel modifications using a new Bi/PMMA/TRT interfacial stack (schematic shown in Fig. 1). This semi-automated transfer process utilizes the weakly coupled interface between semimetal Bi and WSe_2 to minimize the introduction of additional defects during the transfer process, while the new PMMA/TRT support stack offers balanced adhesion property and mechanical flexibility to achieve wrinkle-free transfer at large wafer-scale. Atomic force microscopy (AFM, Fig. 2b), and Raman spectrum/photoluminescence (PL) (Fig. 3) were conducted to characterize the surface cleanliness, roughness, and uniformity of the material before and after the transfer process.

B. Devices Fabrication and Charecterization

As described in Fig. 4, after dry-transfer, Helium-ion-beam lithography was used to pattern the S/D contact electrodes. Sb with different thicknesses and Pt capping layers were deposited by e-beam evaporation and followed by lift-off to form the contact electrodes. Then MoO_x and $SiON_x$ were deposited on top as the encapsulating layers, to achieve almost hysteresis-free pFET and nFET, respectively. The I-V characteristics were measured in vacuum system with Keysight B1500A parameter analyzer. Raman spectra was utilized to examine the interface coupling between the contact metal and WSe_2, and energy-dispersive X-ray spectroscopy (EDS) in a scanning transmission electron microscope (STEM) was used to reveal chemical compositions at the contact interfaces.

III. Results

A. Sb-Pt Contact Engineering for WSe_2 p/n FETs

WSe_2 with semimetal contact such as Bi has shown promising nFET device characteristics. To reduce the contact resistance and achieve better WSe_2 pFET performance, it is critical to identify contact metals with appropriate work functions and weaker Fermi-level pinning effect because of metal-induced gap sates (MIGS). We discover that by mixing thin layer semimetal Sb with the high-work-function metal Pt, both issues can be effectively addressed, which offers improved contact and better on-state performance for both nFETs and pFETs made with monolayer WSe_2.

Fig. 5 summarizes typical transfer (I_D-V_G) characteristics of pristine short-channel (L_{CH} = 100 nm) WSe_2 FETs with different Sb and Pt compositions and with Pd contact as the baseline device. Pd is selected as the control material throughout this study because direct deposition of pure Pt on WSe_2 is known to suffer from adhesion issue, and Pd has similar work function as Pt and can serve as good reference. Depending on the Sb-to-Pt ratio, either p-branch current or n-branch current is improved by one and two orders of magnitude, respectively, as compared to the Pd-contact device. It is observed that device with thinner Sb on WSe_2 shows stronger pFET behavior, whereas device with thicker Sb exhibits nFET behavior.

We believe that the Sb-Pt contact plays two vital roles in achieving such improved pFET and nFET performance. First, the insertion of Sb provides a buffer layer in between WSe_2 and the high-work-function Pt metal, which minimizes lattice damage to WSe_2 during Pt metal deposition, and alleviates the metal-WSe_2 interactions. To confirm this effect, Sb/WSe_2 and Pd/WSe_2 reference heterostructure samples are prepared for Raman spectroscopy measurements [6], and the results are presented in Fig. 6. The Raman characteristic peak of WSe_2 becomes wider and much weaker after 1.5 nm Pd is deposited on top. The Pd/PMMA/WSe_2 sample displays a similar Raman intensity to the pristine WSe_2 sample, ruling out the possibility that 1.5 nm Pd may block the incident light and attenuate the local light field on WSe_2 during the Raman spectroscopy measurement. Hence, some level of disruption of the WSe_2 lattice is induced after the deposition of conventional high work-function metals such as Pd, possibly through defect introduction or interfacial chemical bonding. Both effects can lead to severe Fermi-level pinning effects, including defect induced gap states (DIGS) and MIGS. By contrast, the Raman peak of Sb/WSe_2 sample do not exhibit any intensity or width change, indicating less disruption caused to the WSe_2 lattice by semimetal Sb than Pd.

Second, the interfacial properties, especially the effective work functions at the Sb-Pt/WSe_2 interfaces can be modulated by the Sb-to-Pt ratio, which contributes to the nFET-to-pFET conversion. Cross-sectional STEM images and the corresponding EDS mappings on the Sb/Pt contact regions of WSe_2 FETs are shown in Fig. 7. It is worth noting that partial re-sublimation of Sb may take place during the Pt evaporation because of heating, resulting in slightly smaller thickness of the actual Sb layers than the target deposition thickness. Another interesting observation is that mixing between Sb and Pt may occur at the metal/WSe_2 interface especially when thinner Sb (10 nm) is deposited (Fig. 7 b and c). The Sb-Pt mixing can modulate its effective work function, and thus the contact barrier at the metal/WSe_2 interface. Note that the work function of pristine Sb and Pt are 4.4 eV and 5.6 eV, respectively, and the Sb-Pt mixed layer could have an effective work function in between, which can result in the polarity modulation of the WSe_2 FETs when the deposition thickness of Sb changes.

Fig. 8 and 9 show the output (I_D-V_D) characteristics of the best nFET and pFET for pristine WSe_2 with Sb 10 nm/Pt 12 nm and Sb 30 nm/Pt 12 nm as the contact electrodes, respectively. The relationship between the p-branch and n-branch on-currents and the different Sb/Pt compositions are summarized in Fig. 10.

B. p/n FET Performance Boosting with Channel Modulation

To further boost the on-state current for both the pFETs and the nFETs, we capped the WSe_2 channels with different dielectric layers: 10 nm MoO_x deposited by e-beam evaporation for pFETs, and 30 nm $SiON_x$ deposited by atomic layer deposition (ALD) for nFETs. The presence of capping layers leads to two beneficial impacts: (i) interface trap states passivation, and (ii) modulation doping. First, the capping layers are able to neutralize the trap states, making the device characteristics almost hysteresis-free (Fig. 11). Second, modulation doping as well as an enhancement of on-state currents can be induced by the MoO_x and $SiON_x$ capping layer for pFET and nFET, respectively.

After Sb-Pt contact engineering and capping layer engineering, we report high-performance I-V characteristics for both nFET and pFET with monolayer WSe_2. The output characteristics for the 1L WSe_2 pFET and nFET are shown in Fig. 12 and Fig. 15, respectively. The on-state current for pFET (contact metal: 10 nm Sb/12nm Pt; capping: 10 nm MoO_x) is 151 μA/μm (V_D = -1 V) and the on-state current for nFET (contact metal: 30 nm Sb/12nm Pt; capping: 30 nm $SiON_x$) is 147 μA/μm (V_D = 1 V).

C. Contact Resistance and Schottky Barrier Height

Both Y-function method (YFM) and transfer-length method (TLM) are used to estimate the contact resistances of the optimized 1L WSe_2 pFET and nFET (Fig. 13, 14, and 16). According to YFM, the contact resistances R_C are extracted to be 0.9 kΩ·μm for the pFET with MoO_x capping, and 1.8 kΩ·μm for the nFET with $SiON_x$ capping. In addition, we also employ the TLM method for the pFET to give a more accurate R_C extraction since YFM method typically tends to overestimate the contact resistance. Using TLM, the contact resistance is extracted to be 0.75 kΩ·μm for the 1L WSe_2 pFET.

To extract the Schottky barrier heights Φ_{SB} at the p-type and n-type contacts of the p/n FETs, transfer characteristics are measured at different temperatures (from 100 K to 300 K), as plotted in Fig. 17. It is observed that the drain currents for both the pFET and the nFET decrease at lower temperature, which suggest that the transport characteristics for both devices are dominated by the Φ_{SB} at the metal contacts. Φ_{SB} can be extracted by finding the slopes of the Arrhenius plots ($\ln(I_D/T^{1.5})$ versus 1/T) as shown in Fig. 18 (a). The Φ_{SB} as functions of the gate voltage for the pFET and the nFET are summarized in Fig. 18 (b), which is the comprehensive result after considering the barrier width change caused by doping effect. Using this novel Sb-Pt modulated contact technology, the contact barriers are small for both pFET and nFET at room temperature.

D. Benchmark

Fig. 19 and 20 benchmark the I_{ON} as a function of channel length among our work and previous studies of monolayer CVD and exfoliated WSe_2 FETs [7-17]. The on-state current for both our pFET and nFET are among the highest reported in the literature with the nFET current being record value among CVD 1L WSe_2 nFET. Our reported pFET R_C is the lowest among all monolayer 2D pFETs while the nFET R_C is also the lowest among 1L CVD WSe_2 nFETs, as shown in Fig. 21. These devices exhibit high performance and low contact resistance with minimal hysteresis for both pFETs and nFETs, and are hence a promising technology for developing WSe_2 FETs toward 2D CMOS electronics for advanced logic.

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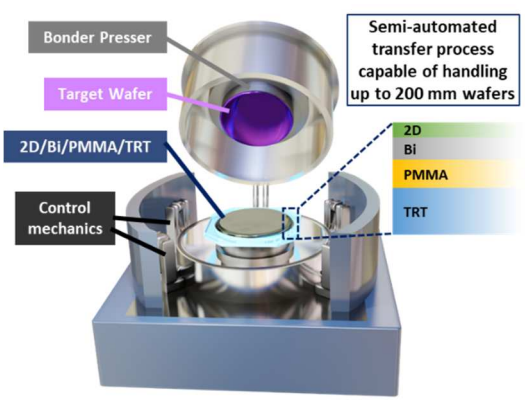

Fig. 1. Schematic of the Bi-assisted semi-auto transfer facility capable of handling up to 200 mm wafers. The technology is further improved in this work by using thermal release tape (TRT) and PMMA to enhance transfer quality.

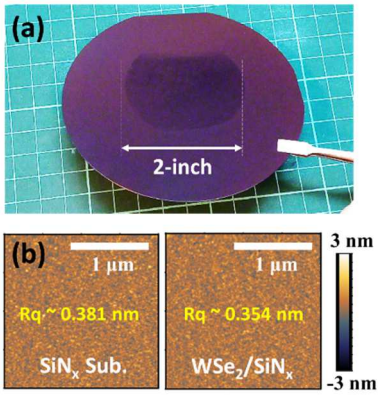

Fig. 2. (a) Photograph of 2" CVD-1L-WSe_2 transferred on 4" SiN_x (100 nm)/p^{++}-Si wafer. (b) AFM images of the SiN_x/Si substrate alone and after WSe_2 film is transferred, showing comparable surface roughness.

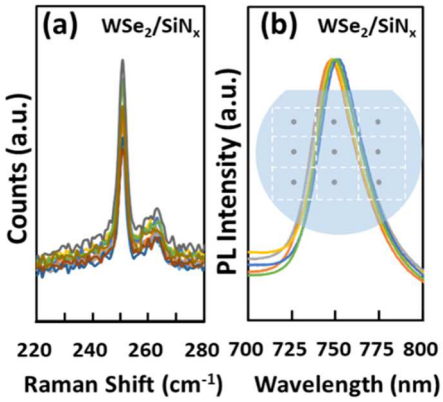

Fig. 3. (a) Raman and (b) PL spectra of the transferred WSe_2 on SiN_x/Si substrate, showing uniform Raman and PL peak positions at all nine locations of the 2" region in Fig. 2(a), demonstrating the uniform quality of the transferred WSe_2 material.

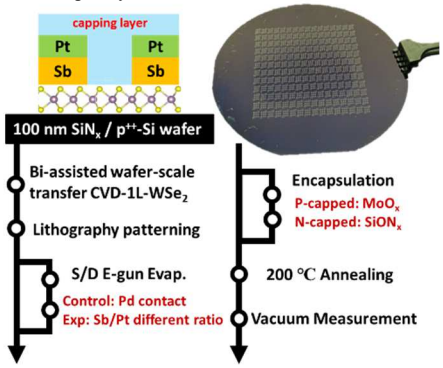

Fig. 4. Key process steps and schematic diagram of the back-gated CVD 1L-WSe_2 device fabrication with contact metal and encapsulation splits. Photo of the wafer after device fabrication is also shown.

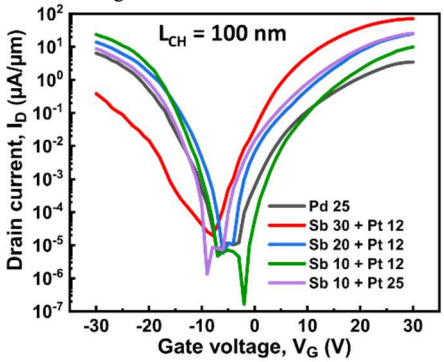

Fig. 5. Transfer characteristics (I_D-V_G) of the Pd-contacted and different compositions of Sb/Pt-contacted 1L-WSe_2 FETs at $|V_D| = 1V$. The device characteristics without encapsulation are ambipolar.

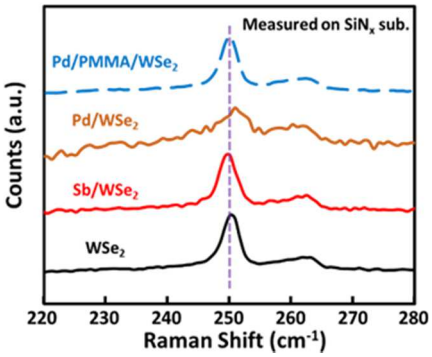

Fig. 6. Raman spectra of pristine 1L-WSe_2, and those capped with 1.5 nm Sb, Pd, and Pd/PMMA. WSe_2 Raman peak becomes distorted in the sample directly capped with Pd, but remains intact in the Sb capped sample.

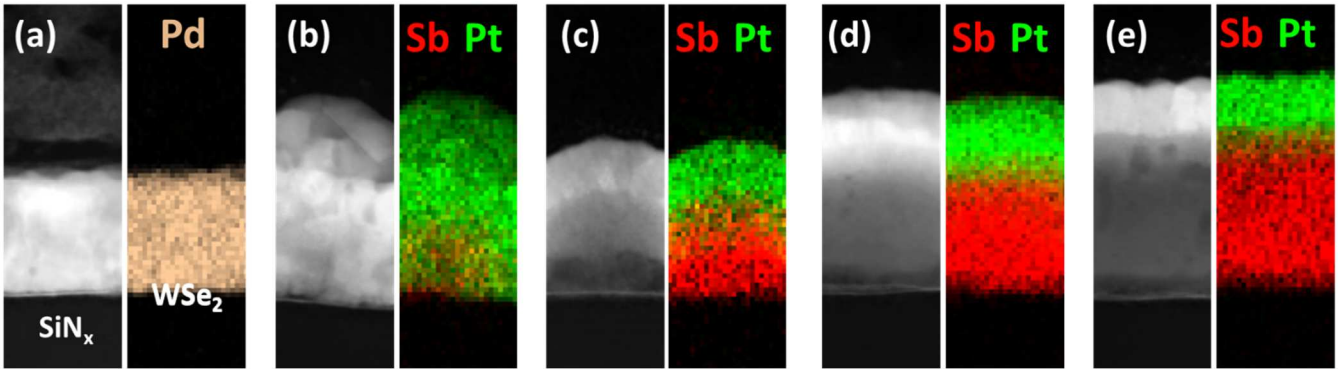

Fig. 7. High resolution cross-sectional STEM images and EDS mapping of (a) Pd. Pd is selected as the control p-type contact material because direct deposition of pure Pt on WSe_2 is known to suffer from adhesion issue, and Pd has similar work function as Pt and can serve as good reference, and (b-e) different compositions of Sb/Pt contacted on 1L CVD WSe_2. Note: (b) 10 nm Sb with 25 nm Pt, (c) 10 nm Sb with 12 nm Pt, (d) 20 nm Sb with 12 nm Pt, (e) 30 nm Sb with 12 nm Pt. Thinner Sb intermixes more vigorously with Pt, resulting in more complete alloying of Sb and Pt.

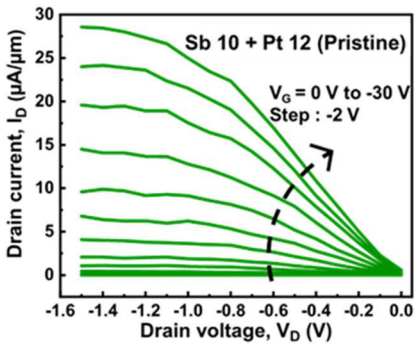

Fig. 8. Output characteristics (I_D-V_D) of 1L-WSe_2 pFET (L_{CH} = 100 nm) with 10 nm Sb + 12 nm Pt of S/D contacts.

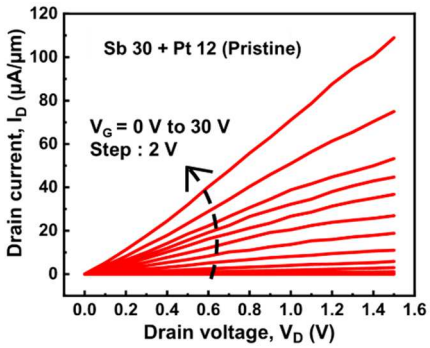

Fig. 9. Output characteristics (I_D-V_D) of 1L-WSe_2 nFET (L_{CH} = 100 nm) with 30 nm Sb + 12 nm Pt of S/D contacts.

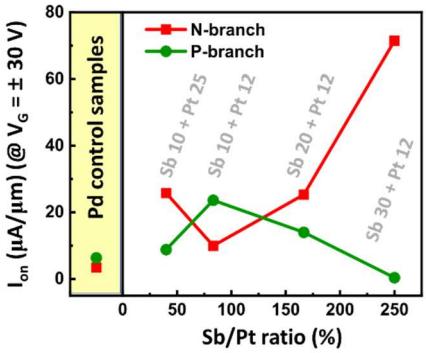

Fig. 10. Changes in the p/n FETs performance with different contact compositions. 10 nm Sb + 12 nm Pt contact gives the best pFET performance.

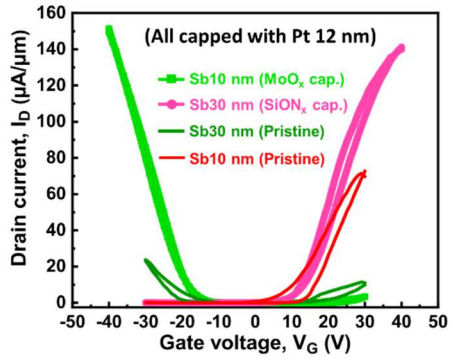

Fig. 11. Transfer characteristics (I_D-V_G) of the Sb/Pt-1L-WSe_2 FET (L_{CH} = 100 nm) at $|V_D|$ = 1 V, before and after MoO_x (Green) and $SiON_x$ (Pink) encapsulation.

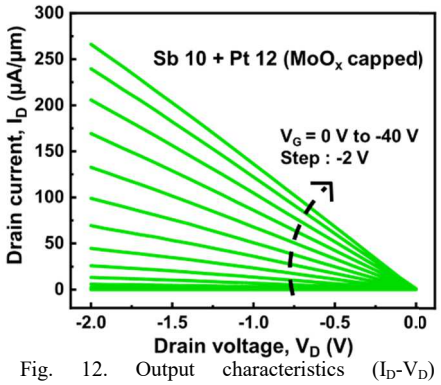

Fig. 12. Output characteristics (I_D-V_D) corresponding to bright-green-line in Fig. 11, i.e. Sb/Pt:10/12 nm after MoO_x capping.

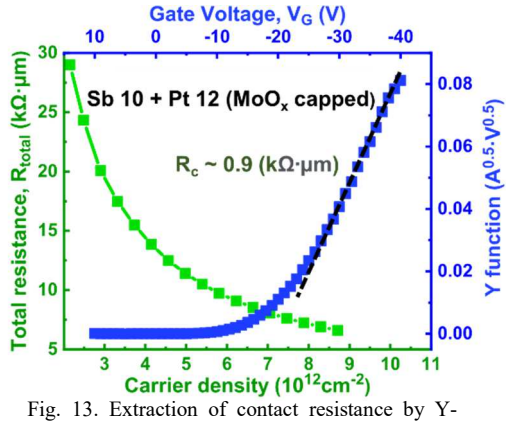

Fig. 13. Extraction of contact resistance by Y-function method for the Sb10Pt12-WSe_2-pFET after MoO_x capping.

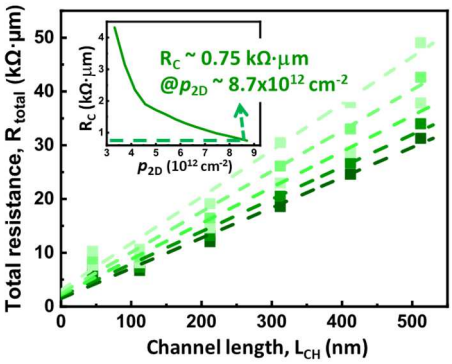

Fig. 14. Extraction of R_C by TLM analysis for the MoO_x capped 1L WSe_2 pFET with carrier density modulated by the gate. R_C = 0.75 kΩ·μm is extracted at carrier density p_{2D} ~ 8.7x10^{12} cm^{-2}.

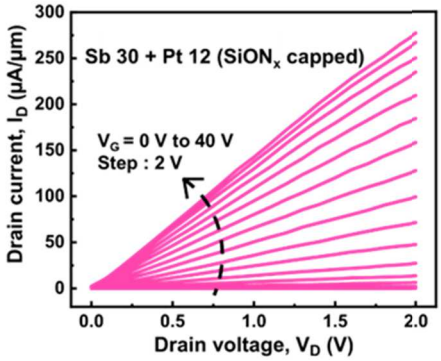

Fig. 15. Output characteristics (I_D-V_D) corresponding to the pink-line in Fig. 11, i.e. Sb/Pt:30/12 nm after $SiON_x$ capping.

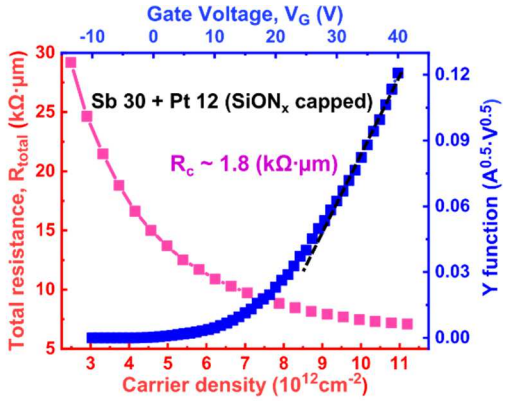

Fig. 16. Extraction of contact resistance by Y-function method for the Sb30Pt12-WSe_2-nFET after $SiON_x$ capping.

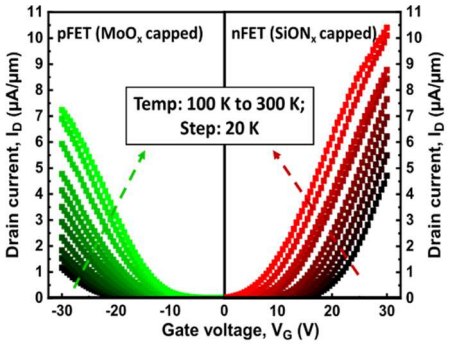

Fig. 17. Temperature-dependent measurement of pFET (Green) and nFET (red). The current levels in both devices decrease at lower temperature.

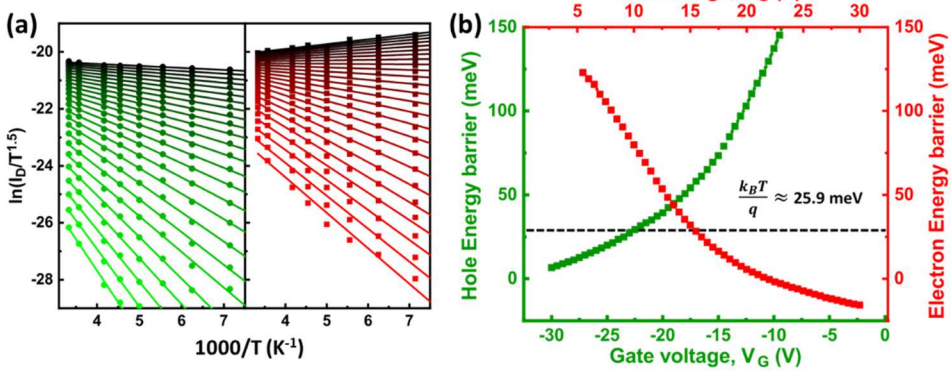

Fig. 18. (a) Arrhenius plots of MoO_x-capped-pFET (green) and $SiON_x$-capped-nFET (red) at different gate overdrive ($|V_G|$ from 6 to 30 V, in step of 1 V). (b) The energy barrier of pFET (green) and nFET (red) are close to be negligible at room temperature. k_B is Boltzmann constant.

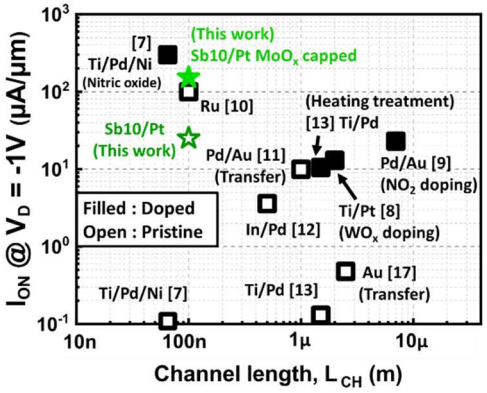

Fig. 19. Benchmark of I_{ON} at V_D = -1 V for 1L WSe_2 pFETs. The open and filled symbols are pristine and doped samples, respectively.

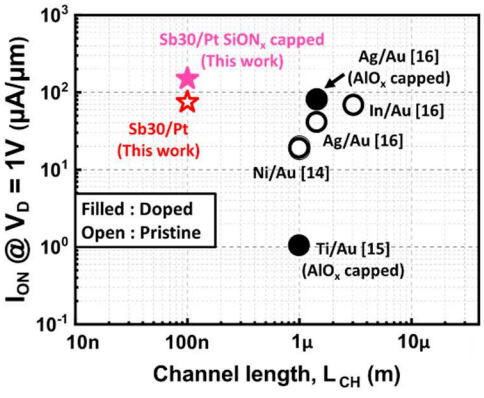

Fig. 20. Benchmark of I_{ON} at V_D = 1 V for 1L WSe_2 nFETs. The open and filled symbols are pristine and doped samples, respectively.

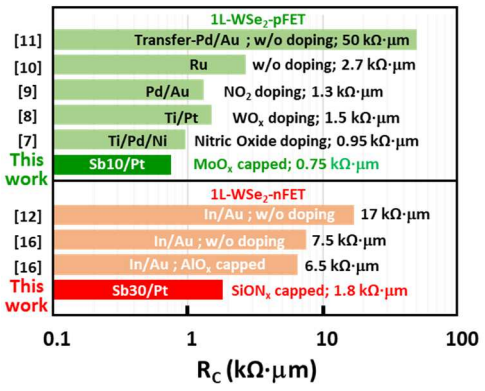

Fig. 21. Comparison of contact resistance for 1L WSe_2 p/n-FETs with respect to different contact approaches reported in the literature.