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Multidimensional device architectures for efficient power electronics

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Power semiconductor devices are key to delivering high-efficiency energy conversion in power electronics systems, which is critical in efforts to reduce energy loss, cut carbon dioxide emissions and create more sustainable technology. Although the use of wide or ultrawide-bandgap materials will be required to develop improved power devices, multidimensional architectures can also improve performance, regardless of the underlying material technology. In particular, multidimensional device architectures—such as superjunction, multi-channel and multi-gate technologies—can enable advances in the speed, efficiency and form factor of power electronics systems. Here we review the development of multidimensional device architectures for efficient power electronics. We explore the rationale for using multidimensional architectures and the different architectures available. We also consider the performance limits, scaling and material figure of merits of the architectures, and identify key technological challenges that need to be addressed to realize the full potential of the approach.

Power electronics technologies provide electrical energy conversion, primarily using solid-state semiconductor devices and passive components. The global power device market reaches US$40 billion (https://www.imarcgroup.com/power-semiconductor-market) and is rapidly expanding, driven by emerging applications such as electric vehicles, data centres, electric grids and renewable energy processing. In power electronics systems, power devices are used as solid-state switches. Ideal power devices should be able to conduct infinite current with minimal resistance, block infinite voltage and switch at infinite frequency with zero power loss. Translated to practical devices, these conditions equate to low on-state resistance (R_{ON}), high breakdown voltage (BV) and small switching losses. The trade-offs between these device metrics usually determine the efficiency, frequency and power density of an entire power electronics system. Thus, innovation in power device engineering is a key driver for energy savings and associated reductions in carbon dioxide emissions.

Power device performance relies on material choice and also device concept and architecture. Conventional power devices—such as the insulated-gate bipolar transistor (IGBT) and the power metal–oxide–semiconductor field-effect transistor (MOSFET)—rely on a semiconductor layer to conduct current and block voltage, and an in-plane gate or base for current modulation. The main current flow and blocking electric field follow the same direction, producing an effective unidimensional (1D) device. These devices are limited by a fundamental trade-off between the volt-ampere capacity and switching frequency of the device (Fig. 1). This is because the conduction and switching losses usually upscale with the conduction current and blocking voltage, and the sum of these losses is inversely proportional to the maximum switching frequency under the system efficiency requirement. For unipolar devices, which switch faster than their bipolar counterparts, there is another strong trade-off between BV and specific R_{ON} ($R_{ON,SP} = R_{ON}A$, where A is the device area)[1]. This trade-off comes from the application of the 1D Poisson theory and reflects the physical origin of the capacity–frequency trade-off for unipolar devices. Such device trade-offs limit a concurrent realization of high power, high frequency, high efficiency and small form factor in power electronics systems.

There are two main approaches to improve these trade-offs in power devices. The first approach is to employ semiconductors with

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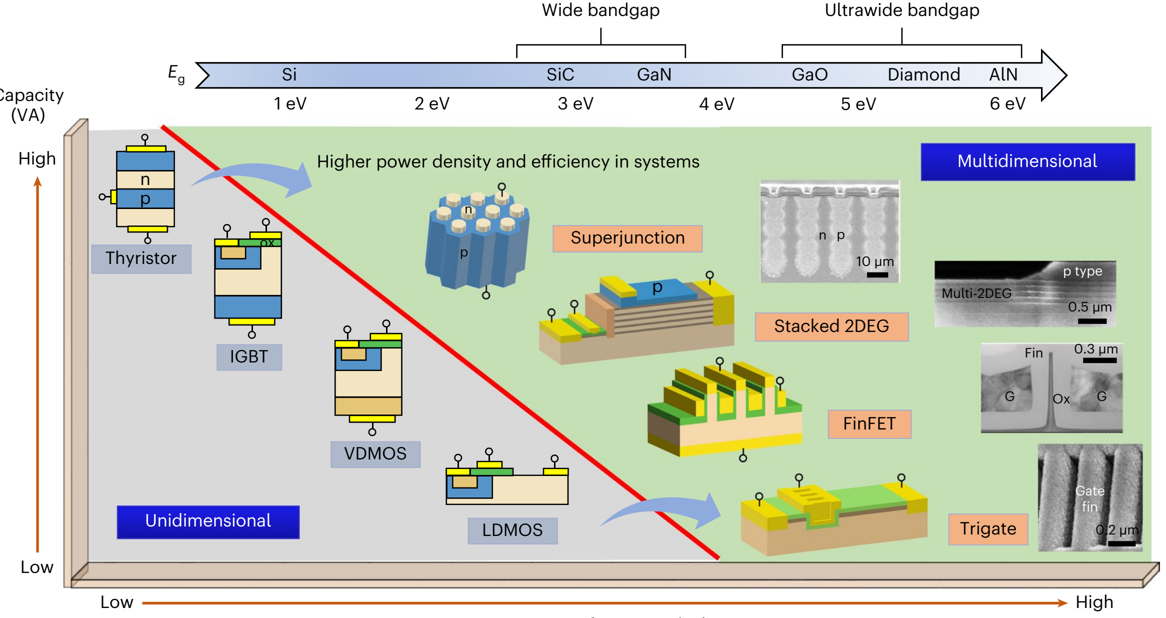

Fig. 1 | Power capacity and frequency trade-off of 1D and multidimensional power devices. The schematic of thyristor, IGBT, vertically diffused MOSFET (VDMOS) and laterally diffused MOSFET (LDMOS) are shown in the left part of the figure. The red line illustrates the approximate limit of 1D power devices. Schematics of a superjunction, multi-channel cascode transistor, Fin-MOSFET and trigate HEMT are presented in the middle part of the figure. The n-type and p-type semiconductors, oxide and metal are plotted in orange, blue, green and yellow, respectively. The circle symbols represent electrodes. The cross-sectional scanning electron microscopy (SEM) images of a silicon superjunction MOSFET, GaN multi-channel transistor, SiC Fin-MOSFET and GaN trigate HEMT are presented in the right part of the figure. The bandgaps (E_g) of silicon and WBG and UWBG semiconductors are illustrated at the top. The multidimensional architectures are material agnostic; their implementations in WBG and UWBG materials can bring advances over the limit of 1D devices. G, gate; Ox, oxide. SEM images, from top to bottom, adapted with permission from: ref. [11], IEEE; ref. [37], IEEE; ref. [40], IEEE; ref. [22], AIP.

superior properties for power switching, such as wide-bandgap (WBG) materials. The last decade has seen WBG devices based on silicon carbide (SiC) and gallium nitride (GaN) reach mass production and commercialization. As the critical electric field (E_C) roughly scales with the square of the bandgap, SiC and GaN—both with bandgaps about three times larger than silicon—can have an E_C that is ten-times higher than silicon. Compared with bipolar silicon devices (such as IGBTs), commercial WBG devices such as a SiC MOSFET and a GaN high-electron-mobility transistor (HEMT) are unipolar and can enable a much higher frequency of operation and provide system benefits[2–6]. Ultrawide-bandgap (UWBG) materials—including gallium oxide (Ga_2O_3), aluminium nitride (AlN) and diamond—are also under development and promise an E_C of at least twice that of SiC and GaN. UWBG devices have a theoretical $R_{ON,SP}$–BV trade-off limit superior to WBG devices[7–10]. However, their current performance is still far below their intrinsic limits due to many material challenges.

The second approach involves innovation in device architecture. The impact of device architecture evolution on power device performance can be seen in the history of 1D silicon power devices before the advent of WBG materials, from the commercialization of thyristors in the 1950s to power MOSFETs in the 1970s to IGBTs in the 1980s. Recently, several innovative architectures have been developed with a common feature of introducing electrostatic engineering in at least one additional geometrical dimension in either the drift or channel region. Superjunctions incorporate the electric-field modulation in a plane perpendicular (transversal) to the current conduction direction, breaking by several orders of magnitude the $R_{ON,SP}$–BV trade-off of 1D devices[11]. The superjunction changed the limit of silicon power devices and has been commercially successful. Another example is to employ a multi-channel stack of two-dimensional electron gas (2DEG) channels displaced in the third dimension (perpendicular to the current conduction plane) in a lateral HEMT structure. This parallel conduction reduces $R_{ON,SP}$ and can push performance beyond the limits of 1D HEMTs. Another example is the use of a fin field-effect transistor (FinFET) and similar multi-gate electrostatics engineering, which create additional dimensions for current modulation in the gated channel. The highly scaled fin-shape channel allows a high channel density and concomitantly results in a shift of the carrier transport towards the path with the highest mobility. The gated channel resistance, which dominates $R_{ON,SP}$ in many conventional device structures, is therefore aggressively reduced.

While the move from planar MOSFETs to multidimensional device structures such as FinFETs has allowed continuous scaling in complementary metal–oxide–semiconductor (CMOS) logic electronics, multidimensional power device architectures can break the trade-off between power capacity and frequency in power devices and systems (Fig. 1). For a given capacity, the $R_{ON,SP}$ reduction allows for smaller A, capacitances and switching losses, and thereby higher frequency (or higher system efficiency at the same frequency). Moreover, this advance is device inherent and applicable to all materials. Such architectures have recently shown encouraging capabilities in silicon, SiC and GaN, and may offer even greater potential in UWBG materials. Moreover, many multidimensional architectures promise improvements to device performance as their sizes are reduced. This is contrary to most 1D unipolar power devices, which are known to gain little improvement with geometrical scaling. This suggests that the current performance limit and figure of merit (FOM) defined for 1D power devices may not be suitable for multidimensional architectures and could underestimate considerably the potential of these device architectures.

In this Review, we explore the potential value of multidimensional architectures in power devices. We consider the rationale for using multidimensional architectures, and the different architectures available: superjunction, multi-channel, FinFET and trigate devices. We

also consider the performance limits, scaling and material FOMs of the architectures, and discuss the critical challenges that lie ahead for the field.

Rationale for using multidimensional architectures

Power transistors are built on a vertical or lateral structure and mainly comprise a gated channel for current modulation and a drift region for voltage blocking. Taking into account the specific resistance of the ohmic contacts (R_C), gated channel (R_{ch}) and drift region (R_{dr}), the theoretical $R_{ON,SP}$–BV trade-off of a 1D vertical unipolar transistor can be written as

$$R_{ON,SP} = R_C + R_{ch} + \frac{4BV^2}{\varepsilon \mu E_C^3} \quad (1)$$

where ε and μ are the material permittivity and majority carrier mobility in the drift region, respectively. Here the R_{dr} limit represents the widely used 1D FOM introduced by Baliga in the 1980s[12]. If the doping dependence of μ and E_C, punch-through design and impact ionization are further considered, the R_{dr} limit is proportional to BV^{α}, in which α ranges from 2.18 (ref. [13]) to 2.5 (ref. [14]).

The R_{ch} of vertical GaN and SiC MOSFETs is limited by the low channel mobility (μ_{ch}) in either the inversion mode or accumulation mode, which could be ten-times lower than in silicon. This is usually believed to be due to interface states (which affects the Columbic mobility) and carrier trapping[3,15]. The highest μ_{ch} reported in SiC and GaN MOS channels is about 130–150 $cm^2 V s^{-1}$ (refs. [3,15]) and about 150–185 $cm^2 V s^{-1}$ (refs. [16,17]), respectively, which are much lower than the bulk mobility of SiC and GaN (about 800–1,200 $cm^2 V s^{-1}$). Limited by μ_{ch}, the smallest $R_C + R_{ch}$ reported in SiC MOSFETs[18] and GaN MOSFETs[16,17] is about 0.65 mΩ cm^2 and 0.45 mΩ cm^2, respectively. In UWBG devices, μ_{ch} is even lower, and it is very challenging to form low-resistance contact[7].

Figure 2a shows the 1D limits of silicon, WBG and UWBG unipolar devices calculated using their material properties[19], the smallest $R_C + R_{ch}$ reported in SiC and GaN MOSFETs, and an optimistic estimation for the $R_C + R_{ch}$ limit of UWBG devices (1 mΩ cm^2). It is evident that $R_{ON,SP}$ of 1D WBG and UWBG devices is dominated by the gated channel at low voltage up to at least kilovolt, from which R_{dr} takes over and the WBG and UWBG material properties can be exploited to improve device performance.

In some materials, such as GaN, R_{ch} can be reduced by using the 2DEG channel in a lateral HEMT, which has a high mobility of about 2,000 $cm^2 V s^{-1}$. The $R_{ON,SP}$–BV trade-off of a 1D HEMT can be written as[20,21]

$$R_{ON,SP} = R_C + R_{CH}\frac{BV}{\eta E_C} + \frac{BV^2}{q n_{2D} \mu_{2D} \eta^2 E_C^2} \quad (2)$$

where q is the elementary charge. n_{2D} and μ_{2D} are the 2DEG concentration and mobility, respectively. ηE_C is the average lateral electric field ($\eta < 1$). R_{CH} is the channel resistivity in Ω mm, and the corresponding R_{ch} (in mΩ cm^2) scales with BV in lateral devices due to the increased device area. Using the typical R_{CH} of p-gate GaN HEMTs[22] and a typical ηE_C of 1 MV cm^{-1} (ref. [23]), the GaN HEMT limit shows advantages over SiC at low voltage (Fig. 2a). This is partly why GaN HEMTs are currently commercialized in the voltage classes lower than SiC.

In addition to the 1D limits, Fig. 2a also shows the state-of-the-art performance of silicon MOSFETs[24], SiC MOSFETs[25], GaN MOSFETs[16,17,26], GaN HEMTs[5], Ga_2O_3 MOSFETs[27,28], AlN/AlGaN HEMTs[29,30] and diamond FETs[31,32]. Lateral GaN HEMTs and vertical SiC MOSFETs are close to their 1D limits, whereas emerging UWBG devices are still far away from their limits as a result of their relative immaturity.

These 1D limits in silicon, SiC and GaN have been recently broken by several multidimensional device architectures, which either alter the R_{dr}–BV trade-off or aggressively reduce R_{ch} (Fig. 2b). A superjunction reshapes the electric field in the drift region and allows for linear dependence of R_{dr} on BV to replace the quadratic limit in equation (1). After reaching a commercial success in silicon[11], a superjunction was recently also demonstrated in SiC, enabling device performance beyond the 1D SiC limit across a wide BV range from 1,170 V to 7,800 V (refs. [33–35]). In the lateral HEMT, the use of stacked 2DEG channels increases the effective n_{2D} without compromising ηE_C due to the balanced polarization charges. Multi-channel GaN HEMTs have been demonstrated beyond the 1D WBG limits with a BV from 1,300 V (ref. [36]) up to 10 kV (ref. [37]).

Channel innovation is essential to enable the benefits of a superjunction and multi-channel to reach low-voltage devices. The use of multi-gate architectures and submicrometre-sized fin-shaped channels can substantially increase the channel density[38], and more fundamentally, shift the carrier transport away from the low-mobility MOS channels[39,40]. This circumvents the μ_{ch} limitation in WBG and UWBG devices. FinFET and trigate devices have been demonstrated in SiC[39–42] and GaN[38], and in both vertical MOSFETs and lateral HEMTs, with the state-of-the-art performance exceeding the 1D R_{ch} limit[19,36,42–44].

The device physics of these multidimensional device architectures is elaborated in the following sections. Interestingly, their performance limits can be continuously enhanced by scaling certain structural parameters, resulting in a new band of device limits beyond the 1D limit line for each power semiconductor material (Fig. 2b). It should be noted that there are other multidimensional structures in power devices. We believe that the three mentioned above are representative as they have enabled device performance to break 1D limits. For example, the junction barrier Schottky diode comprises alternative p-and n-type grids below the contact, which is multidimensional in nature but may be considered as a special form of superjunction that does not possess its full functionality (for example, charge balance) to break the 1D limits.

Superjunction

The $R_{ON,SP}$–BV limit in equation (1) comes from the basic intuition that the higher the resistivity of a drift region (for example, thicker or more lowly doped), the higher the BV. Analytically, this trade-off is described by the solution of the 1D Poisson theory. The field distribution for which the minimum $R_{ON,SP}$ happens has a well-known triangular shape with the maximum electrical field occurring at the junction and the triangular shape filling the drift region at breakdown (Fig. 3a). One can immediately spot that this triangular field shape may not be optimum as the area under the electrical field when the maximum electric field reaches E_C represents the BV. Unfortunately, the only way a rectangle shape can be obtained is by lowering the doping to an intrinsic level, which has the adverse effect of increasing $R_{ON,SP}$ immensely. Therefore the 1D Poisson theory does not result in an ideal field distribution and moreover, the optimal doping is relatively low, thus putting a firm limit on the minimum $R_{ON,SP}$.

The superjunction spectacularly broke the limit of the 1D theory by using a 2D design for which the 1D Poisson limitations no longer apply. The superjunction delivers a rectangular distribution of the electric field in a line across the drift region, and, even more importantly, does so while increasing the doping level by one to two orders of magnitude compared with the 1D design. Figure 3a shows a 1D design, versus a 2D superjunction and a cylindrical superjunction that can be effectively employed in a 3D drift region.

The drift region of a superjunction comprises multiple, alternate n and p semiconductor pillars with relatively high doping. Provided that the pillars are fairly narrow and the net doping charge in the alternate pillars is approximately equal (that is, charge balance), it is possible to deplete such pillars at relatively low voltages applied between the main terminals. Upon depletion, the entire drift region appears to be a single block of 'intrinsic' semiconductor with a near-uniform electric-field distribution. The thinner the pillars, the higher the charge that can be placed inside the n pillars, and therefore the lower the $R_{ON,SP}$ the device

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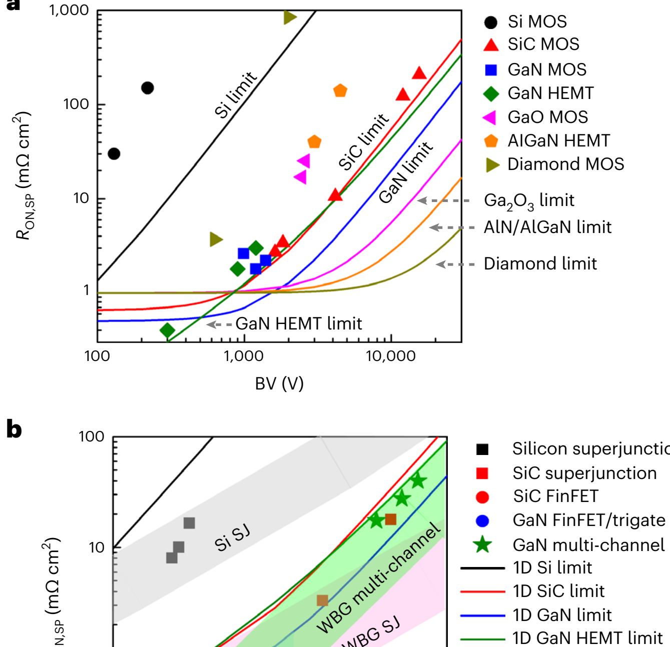

Fig. 2 | Specific on-resistance and breakdown voltage trade-off of 1D and multidimensional power devices. a, $R_{ON,SP}$–BV trade-off of the state-of-the-art silicon MOSFETs, SiC MOSFETs, GaN MOSFETs, GaN HEMTs, Ga_2O_3 MOSFETs, AlN/AlGaN HEMTs and diamond MOSFETs. The 1D limits of silicon, WBG and UWBG vertical unipolar devices and GaN lateral HEMTs are also plotted. The device data are collected from refs. [5,16,17,24–32]. **b**, $R_{ON,SP}$–BV trade-off of the state-of-the-art silicon and WBG multidimensional devices. The device data are collected from refs. [19,33–37,42–44]. The four bands illustrate the performance limits of silicon and WBG superjunction (SJ) devices, WBG multi-channel devices, as well as WBG FinFETs and trigate devices. The geometrical scaling in these multidimensional architectures results in a band of theoretical limits beyond the limit lines of 1D power devices.

can achieve, without compromising the BV. In theory, these pillars can be nanometres in dimensions and the ultimate limitation of their dimension is given by the parasitic junction field-effect-transistor (JFET) effect that appears in the on state. The parasitic JFET effect can be described as a constriction of the on-state current due to the intrinsic depletion generated between the n and p pillars and the additional depletion region created by the application of the drain voltage, which acts as a reverse bias on the p–n junction formed between the pillars[45]. The JFET effect sets a minimum, 'ultimately optimum' width for the superjunction drift region, which is material dependent (elaborated on in section 'Performance limits, scaling and material FOMs')[46,47].

Following the introduction of CoolMOS in 1998[48,49], the superjunction field has delivered some of the best unipolar silicon power devices in the market for the past two decades. The latest silicon CoolMOS has been commercialized from 500 V to 950 V. Figure 3b shows two implementations of a 2D superjunction design in a trench MOSFET. The superjunction pillars can run in the third dimension parallel to the trench width or perpendicular to it[50]. The latter has the advantage that no precise alignment is needed between the superjunction structures and the gated channels. Such design is more appropriate for very narrow superjunction pillars.

The superjunction has been largely described as a silicon concept, as it provided silicon with a tool to fight against the WBG newcomers in the field. However, the superjunction concept is material agnostic and can be employed very efficiently in various forms for SiC and GaN devices. In 2016–2018, SiC superjunction diodes and MOSFETs were first demonstrated with performance beyond the 1D SiC limit at a voltage class around 1.2 kV (refs. [33,51]). The breaking 1D limit performance was later realized in 3.3 kV and 6.5 kV class SiC superjunction MOSFETs[34,35]. In addition to the MOSFETs, the SiC superjunction has also been demonstrated in JFETs recently[52].

The silicon and SiC generations of superjunction structures employed a 2D pillar geometry for the p–n pillars. Owing to its simplicity, this arrangement can be modelled by using 1D Poisson equations applied to two axes (that is, longitudinal and transversal)[11,53,54]. Indeed, several analytical models based on these simplified assumptions have been used to find a limit for $R_{ON,SP}$ with respect to each cell pitch for a given BV[45,53,55–57].

Fujihira's ideal 2D superjunction model unveiled a linear relationship between $R_{ON,SP}$ and BV[53]. Kang and Udrea expanded Fujihira's 2D model, by accounting for the parasitic JFET effect, and derived a new theoretical $R_{ON,SP}$ limit for silicon and WBG superjunctions[46,58]. According to these analytical models, WBG superjunctions possess an optimal cell pitch narrower than the silicon superjunction, as well as higher optimal doping concentration, therefore enabling a much lower $R_{ON,SP}$. This narrower cell pitch can be seen from the cross-sections of experimental silicon and SiC superjunctions (Fig. 3c)[11,59].

Building on the cylindrical superjunction unit cell shown in Fig. 3a, 3D superjunction architectures have been recently proposed and scrutinized for silicon and WBG materials[47]. The 3D superjunction's doping can be increased by a factor of two over that of the 2D structure. This is because, intuitively, the depletion region across the radial p–n junction spreads more extensively than that of stripe pillars, for the same bias condition and doping levels[47]. Figure 3d shows two transistor implementations of a 3D superjunction drift region aligned to the top gated channel[47]. The two show nanowire-style, and nanomesh, shell-style (honeycomb structure) implementations of the n pillars, respectively. For these 3D superjunction transistors, a precise match of size and form factor is not required between the gated channel and the superjunction structure, which can facilitate the geometrical scaling in the superjunction.

Finally, the superjunction can be used as a powerful concept in different types of multidimensional architecture, from 2D extension in the third dimension of n–p stripes or n–p sheet charges in a lateral device[60], to cylindrical n–p stripes between p^+ floating rings in termination regions in a vertical device[61]. Some interesting forms of lateral superjunction are introduced in the next section.

Multi-channel

Multi-channel heterostructures reduce the sheet resistance (R_{SH}) by spreading a large n_{2D} into stacked channels with the n_{2D} in each channel not too high to compromise μ_{2D} due to carrier scattering. The GaN-based multi-channel heterostructures can be either undoped[62–65] or doped[36,43,66,67], and an R_{SH} three- to ten-times lower than the single-channel has been reported in both schemes. In an ideal undoped multi-channel, parallel 2DEGs and two-dimensional-hole gases (2DHGs) with equal n_{2D} are induced on the top and bottom sides of each GaN layer (Fig. 4a). An R_{SH} of 37 Ω sq^{-1} was demonstrated in a 7-channel AlN/GaN heterostructure[63], and a 4-inch, 5-channel AlGaN/GaN wafer is commercially available with an R_{SH} of 115 Ω sq^{-1} (ref. [64]). In contrast, the doped multi-channel usually has impurity[43,67] or modulation doping[66] selectively introduced in each barrier layer to boost 2DEG densities, leaving the quantum well in GaN undoped to minimize the ion scattering and preserve μ_{2D}. An R_{SH} of 67 Ω sq^{-1} was reported in a modulation-doped 8-channel heterostructure[66].

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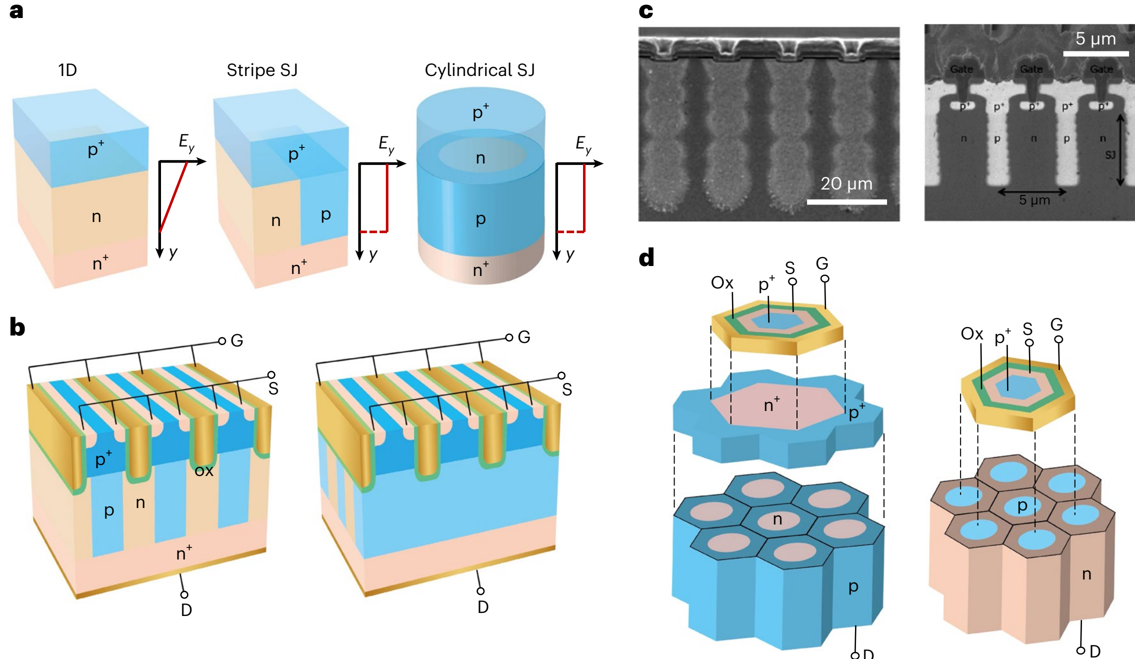

Fig. 3 | Superjunction power devices. a, Schematic of the 1D drift region, 2D superjunction and cylindrical superjunction. The electric-field distribution along the thickness direction (E_y) is illustrated for three drift region designs. **b**, Two implementations of the 2D superjunction trench MOSFET. The superjunction pillars can be parallel to the trench width or perpendicular to it. **c**, Cross-sectional microscopic images of a silicon superjunction (left) and a SiC superjunction (right). S, source; D, drain. **d**, Exploded views of two implementations of the 3D superjunction trench MOSFET. The left device shows a nanowire-style implementation of n pillars in the superjunction, a honeycomb channel unit cell and a current spreading layer in between. The channel unit cell can be larger than the superjunction unit cell, and the current spreading layer connects all n-type nanowires to the gated channel. The right device shows a nanomesh, shell-style implementation of n pillars in the superjunction and a honeycomb channel unit cell. Panel **c** adapted with permission from ref. [11] (left) and ref. [59] (right), IEEE.

Despite the low R_{SH}, multi-channel power devices face major challenges in electric-field management and gate modulation. In the multi-channel drift region, the possible large volume charge would result in a quick drop in electric field and thus a low BV. It was proposed that the undoped multi-channel naturally forms a polarization superjunction, as the precise balance of positive and negative polarization charges on both sides of the GaN layer results in a nearly zero net charge and thus a uniform electric field (Fig. 4b)[62]. For the doped or unintentionally doped multi-channels with net donors, a p-GaN cap layer was proposed to balance these depletion charges in the multi-channel at high voltage, serving as a reduced-surface-field (RESURF) structure (Fig. 4c)[68]. The RESURF is a primitive form of a superjunction based on a 2D curved junction rather than multiple junctions. The double RESURF and multiple RESURF have also proved to be effective in lateral silicon devices[11].

With the natural or p-GaN assisted charge balance, a linear BV increase with the multi-channel length has been demonstrated up to about 10 kV (refs. [62,68]). Figure 4d shows the simulated electric-field contours at high voltage in an undoped multi-channel as well as two doped multi-channels with and without the p-GaN RESURF layer, showcasing the importance of the charge balance (enabled by polarization superjunction or RESURF structure) on enabling a high lateral field strength. This BV scalability with the device length, together with the low R_{SH}, makes the multi-channel architecture an excellent platform for high-voltage devices.

Electric-field management is also critical at the device edge, especially in Schottky barrier diodes (SBDs), as the concurrence of high electric field and parallel current channels could induce a large leakage current. Several effective edge terminations for multi-channel SBDs include the trigate field plate[69], planar p-GaN[64] and junction-fin anode[70]. Leveraging the MOS structure or p–n junction at the planar surface or fin sidewalls, these designs allow the depletion of n_{2D} near the Schottky contact and thus reduce the peak electric field and move it away from the Schottky contact. The p-GaN and junction-fin termination also allow the electric field to spread into p-type materials, further suppressing the field crowding. These terminations enabled GaN multi-channel SBDs to achieve substantial improvements in BV, from 900 V (ref. [69]), to 3.3 kV (ref. [64]), to 5.2 kV (ref. [70]) and ultimately to 10 kV (ref. [68]). The $R_{ON,SP}$ of all these GaN SBDs are two to three times lower than the similarly rated SiC SBDs.

Gate modulation is a pressing challenge for multi-channel transistors, as the indirect gate control over the buried channels results in a deep depletion-mode (D-mode) operation with low transconductance. This is partly why the polarization superjunction HEMTs were demonstrated only on a single 2DEG and 2DHG pair without reaching the multi-channel[71]. Later, the use of a trigate was demonstrated as an effective solution in radio-frequency multi-channel HEMTs, which provides sidewall gate control for the buried 2DEGs[72]. A high-voltage trigate HEMT with an $R_{ON,SP}$ of 0.46 mΩ cm^2 and a BV of 1,300 V was recently demonstrated on a 4-channel doped AlGaN/GaN heterostructure[36]. The enhancement-mode (E-mode) operation was realized by shrinking the fin width to 15 nm. A slanted trigate profile was used in each fin to relax the electric-field stress at the gate edge (Fig. 4e). Similar to n-type transistors, trigate p-type multi-channel HEMTs were also demonstrated with an E-mode operation[73].

An alternative gate design for multi-channel transistors is employing an integrated cascode structure[37] (Fig. 4f). This device monolithically integrates a low-voltage (LV), E-mode HEMT based on a single 2DEG channel and a high-voltage (HV), deep D-mode HEMT based on the multi-channel. The HV-HEMT gate is connected to the LV-HEMT source, forming a cascode configuration, which enables the E-mode operation with the device gate shielded from high voltage

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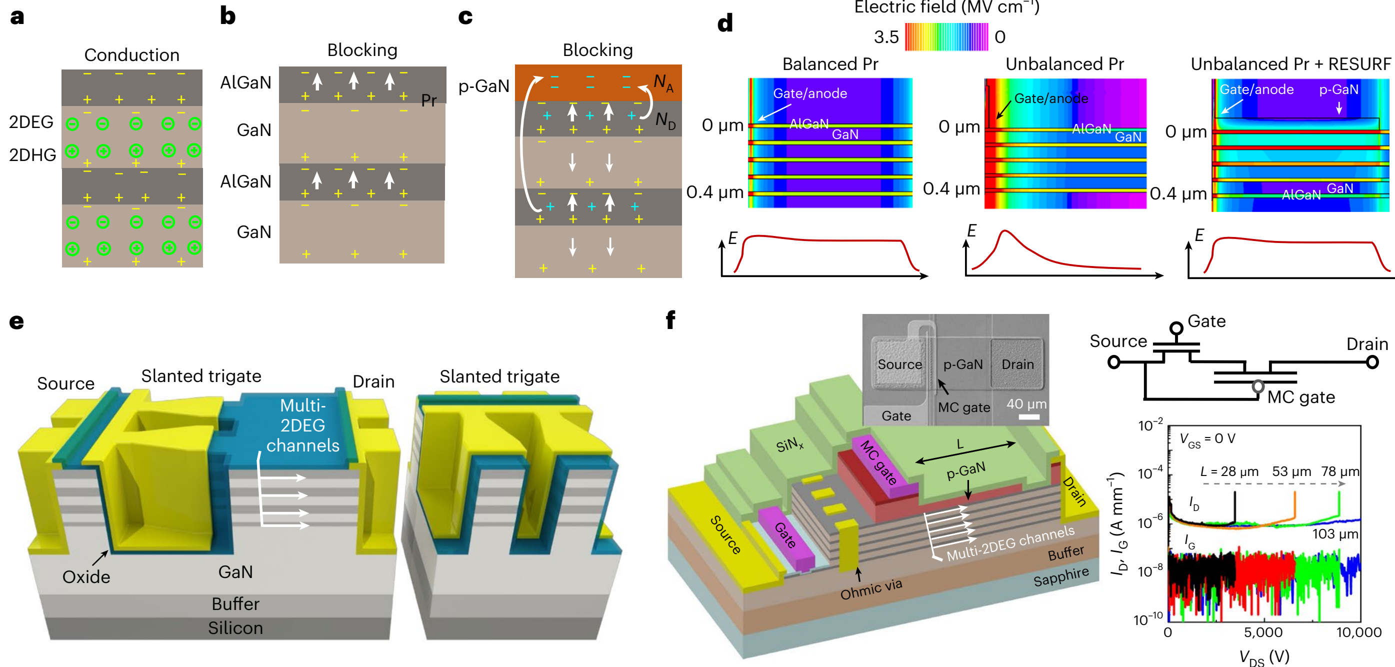

Fig. 4 | Multi-channel heterostructures and multi-channel power HEMTs. a, Illustration of an undoped multi-channel with balanced polarization charges (Pr) in the forward conduction state, in which alternate pairs of 2DEG and 2DHG are formed. **b**, Illustration of an undoped multi-channel with balanced polarization charges in the high-voltage blocking state, forming a polarization superjunction. **c**, Illustration of a doped multi-channel in the blocking state, on top of which a p-GaN RESURF layer provides acceptors (N_A) to balance the net donors (N_D) in the multi-channel. **d**, Simulated electric-field contours in two undoped multi-channels with and without balanced polarization charges, as well as a doped multi-channel with the p-GaN RESURF structure, all at a high blocking voltage. The lateral electric-field distribution is schematically illustrated below each structure. **e**, Schematic of a multi-channel trigate HEMTs with a slanted trigate design. **f**, Schematic, top-view SEM image and the equivalent circuit model of a multi-channel monolithic-cascode HEMT, in which the multi-channel gate (MC gate) is connected to the source. Off-state drain current (I_D) and gate current (I_G) as a function of drain-source voltage (V_{DS}) at zero gate-source voltage (V_{GS}) of devices with different multi-channel lengths (L), showing the scalability of BV to over 10 kV. Panels adapted with permission from: **d**, ref. [68], IEEE; **e**, ref. [36], Springer Nature Ltd; **f**, ref. [37], IEEE.

and high field. By further incorporating a p-GaN RESURF layer, this multi-channel monolithic-cascode HEMT demonstrated a BV up to 10 kV with $R_{ON,SP}$ well below the 1D WBG limits, setting a performance record in multi-kilovolt transistors.

FinFET and trigate

FinFET and trigate devices comprising multi-gate architectures and nanometre-sized fin channels have become the backbone device technology for silicon CMOS electronics at deeply scaled logic technology nodes[74,75]. The fin width of state-of-the-art silicon FinFETs at the sub-10-nm node has been scaled down to 7 nm (ref. [76]). Beyond FinFETs, gate-all-around nanowire and nanosheet FETs are being extensively studied for more advanced technology nodes[76]. These devices show the good success of multidimensional architectures in the digital world.

In the past few years, the FinFET concept has also been leveraged in WBG and UWBG power transistors for two major objectives: (1) realizing a superior gate control and the E-mode operation, exemplified by the trigate multi-channel HEMT discussed in the last section, and (2) increasing channel density and thereby shrinking the R_{ch} that dominates $R_{ON,SP}$ of WBG and UWBG transistors up to the kilovolt voltage class. Other merits reported for power FinFETs included the alleviated current collapse and enhanced thermal management[38]. It is noted that these benefits of FinFET in power are different from those offered to digital electronics. Some benefits of digital FinFETs, such as the low subthreshold swing, enhanced transistor compactness and reduced short-channel effects, are less relevant in the power domain.

A unique feature of power FinFETs and trigate devices that differ from silicon digital FinFETs is a large diversity in the fin body (homo- or heterostructure), device structure (lateral or vertical) and sidewall gate stacks (Schottky, MOS or p–n junction), as shown in Fig. 5. For example, while the fin body is typically undoped in digital FinFETs, the n-type and p-type doping as well as heterojunction-based quantum wells have all been demonstrated in power FinFETs. These structural variations, in conjunction with the fin dimension, result in different carrier profiles and transport characteristics within the fin channel. Below we introduce major power FinFETs and trigate devices as well as their distinct channel electrostatics.

A straightforward approach to reduce R_{ch} using the scaled fins is to increase the channel density without altering the inherent channel electrostatics, as demonstrated in vertical trigate MOSFETs and fin-channel JFETs (Fin-JFETs). SiC trigate MOSFETs employed approximately 0.5-μm-wide fin channels to increase the effective width of the MOS inversion layer, realizing a 3.6-times reduction in R_{ch} and up to a twofold reduction in $R_{ON,SP}$ (ref. [41]). The use of submicrometre fin channels in WBG JFETs has allowed for a shift from the D-mode to E-mode operation[77,78]. As the fin dimension reduces in SiC Fin-JFETs, however, the sidewall ion implantation used for p-gate formation degrades the channel mobility, which offsets the benefits of high channel density and results in a higher R_{ch}. This processing issue is not present for GaN Fin-JFETs owing to their implantation-free fabrication[44]. In conjunction with the fin scaling, GaN fin channels can be doped ten-times higher than the drift region without impairing the E-mode operation, further lowering R_{ch}. An industrial vertical GaN Fin-JFET was demonstrated with an $R_{ON,SP}$ of 0.82 Ω cm^2 and a BV over 1,700 V (refs. [44,78]), rendering the highest FOM in kilovolt-class transistors.

As the fin width scales down to about 200 nm, the E-mode operation can be realized in a junctionless fin owing to the workfunction difference between the gate metal and semiconductor; meanwhile, the junctionless

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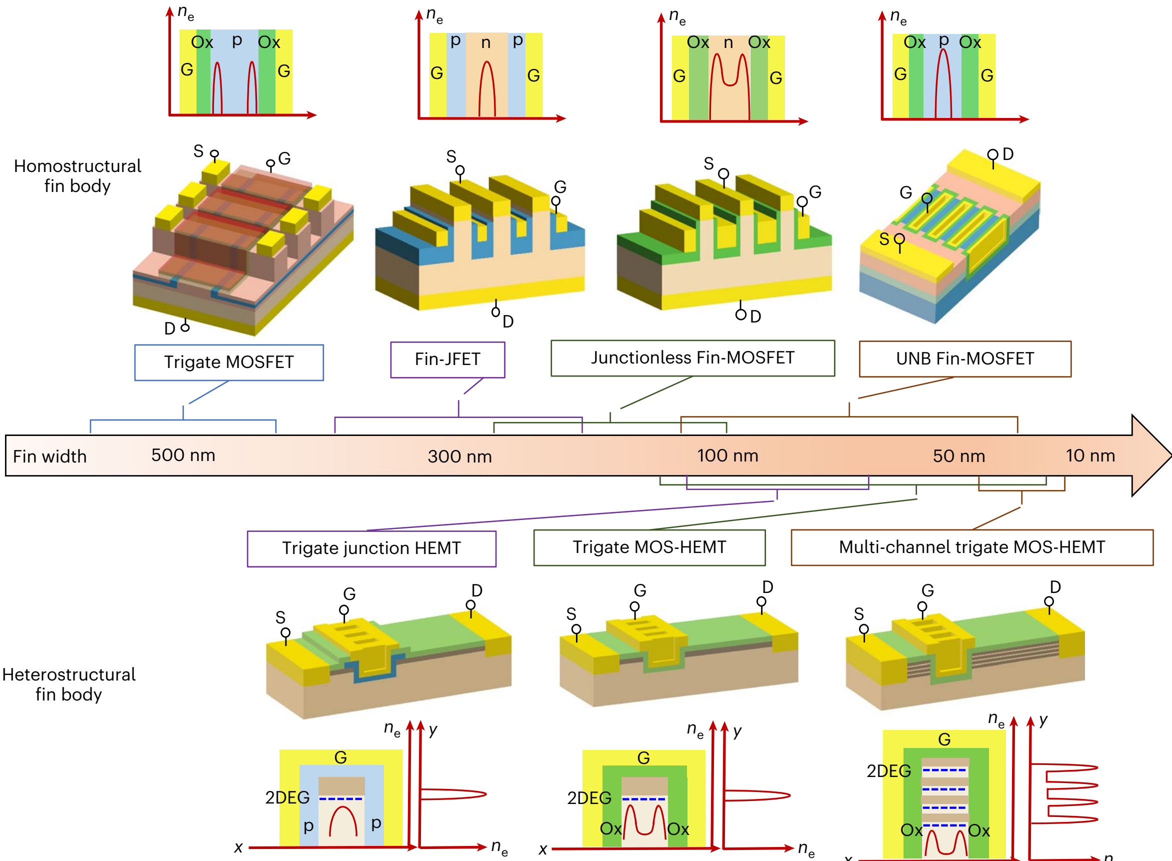

Fig. 5 | Power FinFETs and trigate HEMTs covering a broad range of the fin dimension. Power FinFETs with a bulk fin body are presented above the scale bar. The schematic and channel carrier (n_e) profile of trigate MOSFET, Fin-JFET, junctionless Fin-MOSFET and UNB Fin-MOSFET are shown from left to right. Trigate HEMTs with a heterostructural fin body are presented below the scale bar. The schematic and channel carrier profile of trigate junction HEMT, trigate MOS-HEMT and multi-channel trigate MOS-HEMT are shown from left to right. The approximate fin width range experimentally demonstrated in each device is indicated using coloured curly brackets.

Fin-MOSFET can avoid the punch through up to a kilovolt drain bias at zero gate bias[79]. Such a junctionless fin accommodates two sidewall accumulation-mode MOS channels in parallel with the bulk fin channel, substantially boosting the total carrier concentration and exploiting the higher bulk mobility compared with the MOS mobility[19]. E-mode GaN Fin-MOSFETs with a fin width of about 180–200 nm have been demonstrated, achieving an $R_{ON,SP}$ of 1 mΩ cm^2 (ref. [80]), a BV close to 2 kV (ref. [19]), as well as low junction capacitances and charges[81]. Similar Fin-MOSFETs have also been demonstrated in UWBG Ga_2O_3 with a BV up to 2.6 kV (ref. [27]).

As the fin width further scales to below 100 nm, channel electrostatics become distinct in the inversion-type MOSFET. The inversion layers formed on two sidewalls overlap, forcing the entire fin channel (interface layers and volume) into the strong inversion. This phenomenon is similar to that observed first in low-voltage, double-gate silicon-on-insulator devices[82], the structure of which is similar to FinFETs, and is known as the 'volume inversion'. Due to this effect, carrier transport is shifted to the centre of the fin, allowing the full exploitation of the higher bulk mobility. The fabricated ultra-narrow-body (UNB) SiC MOSFETs with 55-nm-wide fins show a channel mobility of 276 cm^{-2} V^{-1} s^{-1}, which is 10-times higher than that in conventional SiC MOSFETs[39]. Further studies revealed that the FinFET effect can allow for up to an 18-times increase in channel mobility[40]. A fin-width window of about 30–50 nm is predicted to be optimal for UNB SiC MOSFETs[40]. The FinFET effect has also been leveraged to demonstrate a vertical SiC FinFET with an $R_{ON,SP}$ of 0.7 Ω cm^2 and a BV over 1,000 V (ref. [42]).

When the FinFET concept is brought into HEMTs, the heterostructure fin is wrapped by the gate stack, forming a trigate control over the 2DEG channel. In AlGaN/GaN HEMTs, this narrow fin reduces the piezoelectric polarization and 2DEG density due to the partial strain relaxation in the AlGaN barrier[83], facilitating the E-mode realization. Compared with other E-mode gate structures, trigate HEMTs retain high n_{2D} and μ_{2D} and allow for a lower gate channel resistivity[22]. The early power trigate HEMTs in GaN were demonstrated based on Schottky-type gates[84]. Later, the MOS gate stack became the prevailing choice in GaN trigate HEMTs, as it reduces the gate leakage current and increases the gate overdrive range[85]. A critical trade-off of these trigate HEMTs lies between n_{2D} and the fin width needed for realizing the E-mode operation. A fin width down to about 20–30 nm is usually required for achieving the E-mode operation in trigate GaN MOS-HEMTs[38]. This requirement could be relaxed to 100–200 nm if an additional barrier recess[85] or a trap charge oxide[86] is employed, or it could be tightened to below 15 nm for multi-channel trigate MOS-HEMTs[36].

Similar to Fin-JFETs, a junction trigate HEMT was recently demonstrated with a p–n junction wrapping around the heterojunction fins in the gate region[22]. Owing to a higher built-in potential of the p–n junction, the junction trigate provides a stronger depletion, enabling the E-mode operation with a fin width over 60 nm (ref. [22]). This stronger depletion in the junction trigate also minimizes the short-channel effects, particularly at high temperatures, enabling the demonstration of kilovolt blocking capability at 150 °C in GaN trigate HEMTs[87]. More interestingly, the junction trigate congregates the 2DEG towards the centre of the fin body, and therefore, enables higher effective mobility and lower gate capacitance compared with the MOS trigate, in which the 2DEG density usually peaks near the sidewall[87].

Table 1 | Performance limit, scaling parameter and limit, minimum specific on-resistance, and material FOM of 1D vertical unipolar devices, 2D and 3D superjunction devices and the multi-channel lateral devices with precisely matched polarization charges

Drift region design	1D	2D superjunction	3D superjunction	Multi-channel (PSJ)
Structure	S G D	n p ... d	r βr n p	... N channels
Performance limit	$R_{ON,SP} = \frac{4}{\varepsilon\mu E_C^3}BV^2$	$R_{ON,SP} = \frac{4d}{\varepsilon\mu E_C^2}BV$	$R_{ON,SP} = \frac{r}{\beta\varepsilon\mu E_C^2}BV$	$R_{ON,SP} = \frac{BV^2}{NqE_C^2 n_{2D}\sum_{e,h}\mu_{2D}}$
Scaling parameter	NA	Cell pitch (d)	Radius (r), radius ratio (β)	Channel number (N)
Scaling limit	NA	$d = \frac{50E_g}{9qE_C}$	$r = \frac{98\sqrt{2}E_g\beta}{27qE_C}$	Process and technology related
Minimum specific on-resistance	$\frac{4BV^2}{\varepsilon\mu E_C^3}$	$\frac{20E_g BV}{q\varepsilon\mu E_C^3}$	$\frac{16E_g BV}{q\varepsilon\mu E_C^3}$	–
Material FOM	$\varepsilon\mu E_C^3$	$\varepsilon\mu E_C^{2.5}$	$\varepsilon\mu E_C^{2.5}$	$E_C^2 n_{2D}\sum_{e,h}\mu_{2D}$

ε is permittivity, μ is the mobility of the major carrier, E_C is critical electric field, n_{2D} is 2DEG or 2DHG density, μ_{2D} is 2DEG or 2DHG mobility, e and h refer to the electron and hole, respectively, q is the elementary charge, and E_g is the bandgap. PSJ, polarization superjunction; NA, not available.

Performance limits, scaling and material FOMs

Power loss occurs during the device conduction and switching as well as at its gate driver. It is thus dependent on switching scheme and circuit topology. A few device-level FOMs (DFOMs) that incorporate R_{ON}, which determines the conduction loss, and the switching/driver-related device parameters, are routinely used for device selection in various applications[88]. In hard switching, voltage and current waveforms intersect during the time of device transition between on and off states. For fast switching with minimal circuit parasitic, the hard-switching loss in each cycle approaches the energy stored in the device output capacitor[89,90], which is related to the output charge (Q_{OSS}). Hence, $R_{ON}Q_{OSS}$ is widely used as a DFOM for hard switching. By contrast, soft switching enables a nearly zero switching loss by minimizing voltage–current intersections, leaving only R_{ON} to dominate the device loss. Finally, the driver loss is related to the gate charge (Q_G) that needs to be supplied or extracted for device turn on and off. Hence, $R_{ON}Q_G$ is a DFOM relevant for applications where the driver loss is considerable, such as the high-frequency driving.

The $R_{ON,SP}$–BV trade-off is an overarching limit for most DFOMs. $R_{ON,SP}$ not only determines R_{ON} but also impacts Q_{OSS} and Q_G, as for the same R_{ON}, the device with lower $R_{ON,SP}$ has a smaller A, and generally, smaller charges. In particular, this trade-off dictates the device performance limit in soft-switching applications with small driver loss. To this end, in this section, we first discuss the $R_{ON,SP}$–BV trade-off and then revisit $R_{ON}Q_{OSS}$ and $R_{ON}Q_G$ for multidimensional devices.

As illustrated earlier, for conventional 1D vertical devices, if contact and channel resistances are neglected, the $R_{ON,SP}$ limit is proportional to BV^2 with their ratio only dependent on material properties. This relation no longer holds for multidimensional devices. As shown in Table 1, the $R_{ON,SP}$–BV limits of 2D and 3D superjunction devices[46,47] as well as multi-channel devices (with naturally balanced polarization charges) hinge on not only material properties but also device geometries, for example, superjunction cell pitch (d or r), radius ratio (β) and channel number (N). In these devices, the electrostatics in the additional dimension breaks a new path beyond the material innovation for advancing the device performance.

The performance limits of 2D and 3D superjunctions can be continuously advanced by downscaling the cell pitch, and this scaling is typically limited by the process technology available. An additional geometry parameter, β, can be also downscaled in 3D superjunctions to improve the device performance. Recently, it was found that this geometrical downscaling cannot continue indefinitely and, by accounting for the parasitic JFET effect, there is a material-dependent intrinsic limit being no longer related to geometry (and technology)[46]. The minimum cell pitch is inversely proportional to the bandgap of semiconductor materials, for example, around 180 nm, 50 nm and 40 nm for 2D superjunctions based on silicon, SiC and GaN, respectively, and the ultimate minimum $R_{ON,SP}$ is only material dependent. A material FOM can be therefore defined to describe the material limit of superjunction performance, as shown in Table 1. This new FOM is proportional to $E_C^{2.5}$, while the 1D FOM is proportional to E_C^3.

The $R_{ON,SP}$ limit of ideal lateral multi-channel devices is proportional to BV^2, which is similar to 1D devices but different from superjunction devices (proportional to BV). In theory, this limit can be indefinitely downscaled by increasing the number of channels. A merit of the multi-channel with naturally balanced polarization charges is the almost zero vertical electric field in each channel layer (for example, GaN layer in the AlGaN/GaN structure; Fig. 3d), allowing for a lateral field near E_C. The practical scaling limit of channel numbers could be more process related, for example, challenges in contact and gate formation, than material related, particularly if the lattice-matched heterostructure is used to minimize epitaxial challenges[91]. The material's FOM is proportional to E_C^2 as well as the density and mobility of the 2DEG and 2DHG. It is worth noting that the vertical polarization superjunction with heterostructure pillars has also been studied theoretically[92,93]; its performance limit and material FOM are similar to 2D superjunctions but distinct from the lateral multi-channel devices.

The hard-switching DFOM, $R_{ON}Q_{OSS}$, has been recently analysed for 2D superjunctions[94]. While $R_{ON,SP}$ can be continuously reduced by scaling d and increasing the doping concentration accordingly, the price it has to pay is the increased specific Q_{OSS}. The $R_{ON}Q_{OSS}$ limit of the 2D superjunction, $2BV^2/\mu E_C^2$, turns out to be d independent and less than two-times lower than the limit of 1D devices, $4BV^2/\mu E_C^2$ (note that the mobility μ in superjunction is usually lower than 1D devices due to a higher doping concentration). Although no quantitative $R_{ON}Q_{OSS}$ modelling of 3D superjunction and multi-channel devices have been reported, a similar increase in specific Q_{OSS} along with the $R_{ON,SP}$ downscaling could be expected, which may result in a $R_{ON}Q_{OSS}$ independent of the scaling parameter. This suggests that soft switching circuit topologies are preferable to exploit the inherent performance superiority of multidimensional devices.

Similar to the scaling effect in superjunction and multi-channel devices, geometrical scaling is expected to be also preferable in FinFET

and trigate architectures to enable continuous R_{ch} reduction. The design of fin-based gates centres on concurrently realizing the E-mode operation, increasing the channel density and tuning the carrier transport towards the higher-mobility body region. The downscaling of the fin width is beneficial to all three of these design objectives. In contrast, Q_G of a power transistor usually consists of gate-to-source charge (Q_{GS}) and gate-to-drain charge (Q_{GD}), which depends not only on the gate structure but also on the drift region. For example, the Q_{GD} limit of a planar gate superjunction MOSFET hinges on the gate oxide capacitance and superjunction pitch width[94]. This coupling effect suggests that the Q_G optimization for fin-based gates may require a co-design between gate and drift region. Further investigations are desired to explore the scaling laws of R_{ch} and Q_G as well as the associated material FOMs for the diverse fin gates in power devices.

Multidimensional architectures in radio-frequency devices

Over recent decades, radio-frequency electronics is another field that has witnessed the success of WBG devices. Despite the distinct operation principles of radio-frequency and power devices (function as amplifiers and switches, respectively), they share some common device platforms and structural concepts (for example, HEMT). Emerging radio-frequency applications, such as 5G communications, are migrating to millimetre-wave frequencies and require concurrent advancements in the power, frequency and dynamic range of radio-frequency transistor technologies. Multidimensional architectures have been recently introduced to radio-frequency devices to achieve these targets[95]. Hence, it is interesting to briefly mention these multidimensional radio-frequency devices.

Parasitic capacitance is the key limiting factor for upscaling the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of radio-frequency transistors, and it usually increases with device area. The superjunction and multi-channel structures can maximize the chip real estate utilization to boost the blocking voltage and conduction current, potentially breaking the power–frequency trade-off of conventional radio-frequency transistors. For example, excellent trade-offs between f_T, f_{max} and BV were reported in silicon superjunction MOSFETs[96]; trigate multi-channel GaN HEMTs showed higher current and power densities compared with their single-channel counterpart at 30 GHz (ref. [97]). The incorporation of a top p-diamond RESURF layer for this multi-channel GaN HEMT achieved a further capacitance reduction and BV enhancement[98].

Linearity is a key metric of radio-frequency transistors that determines their dynamic range, which could also be improved by the deployment of multidimensional structures. Due to the presence of multiple channels, the transconductance (g_m) of multi-channel HEMTs was found to exhibit broad plateau characteristics, which lead to higher device linearity[38,97]. In single-channel HEMTs, a linearized and broad g_m plateau was realized by using a trigate comprising multiple fins with variable widths[99,100]. These channels and fins in the additional dimension provides the new flexibility to tune the device radio-frequency characteristics.

Outlook

Multidimensional architectures in silicon, SiC and GaN power devices have advanced rapidly over the past two decades. State-of-the-art multidimensional devices have broken the 1D unipolar limits over a wide range of voltages—from 100 V to 10,000 V—and shown encouraging capabilities in terms of power capacity, frequency, efficiency and form factor of power electronics systems. Due to their electrostatics in additional dimensions, these architectures enable new material FOMs and device scaling theories for power devices. Thus, power device advancement is envisioned to no longer solely rely on material innovation.

Further efforts in physics, material science, devices, processing technologies, packaging and circuits are however needed to push multidimensional power devices towards their limits. Many knowledge gaps exist in the fundamental electrical and thermal transport properties within multidimensional devices. For example, a strong thermal interaction between the 3D gate and multi-channel was recently revealed[101] and electric-field mapping and imaging[102] are also desirable to help further visualize the electrostatics in multidimensional structures. From a material standpoint, the use of multidimensional architectures in UWBG devices promises a further performance leap, but the relevant demonstrations are still in their infancy.

Another key area of development is the switching characteristics of multidimensional architectures, particularly at high frequency. For example, interesting dynamic phenomena such as output capacitance hysteresis[103] have been reported in superjunction devices and the inter-fin design in FinFETs, which is not critical for $R_{ON,SP}$ and BV, has been found to play a determining role in the switching speed and losses[104]. Reliability and robustness are also important aspects of these devices and work in this area is increasing with reports looking at their avalanche and short-circuit robustness[105–107], gate reliability and stability[108], as well as the cosmic-ray robustness[109].

A recent example illustrates valuable robustness characteristics enabled by multidimensional device architectures where a GaN Fin-JFET was used as an avalanche GaN transistor[78]. Its avalanche current could flow through either the p-type gate or the n-type fin, depending on whether the gate was off or on[110]. With the gate on, a GaN Fin-JFET shows a unique short-circuit capability at breakdown voltage[105], and it fails with an open-circuit signature due to the spatial separation of electric field and current stresses, which is desirable for module and circuit safety[106]. By contrast, most other types of power transistor fail short-circuit and cannot survive the concurrence of avalanche and short-circuit currents.

While multidimensional devices offer a breakthrough trade-off between the power capacity and frequency, the driving circuitry and heat extraction are key to exploiting their full capabilities in power electronics systems. To minimize circuit parasitics and to allow for high-temperature operation, monolithic WBG and UWBG integrated circuits are desirable for device drive and control[111–113]. Power devices and integrated circuits could also share the same multidimensional device platform. For example, Intel recently demonstrated the monolithic integration of GaN power FinFETs and GaN n-channel digital FinFETs, where the latter is 3D stacked with a silicon p-channel digital FinFET to form GaN–Si CMOS for driving circuitry[114]. Finally, due to a higher power density, the device packaging and thermal management will be important, and a device-package, electrothermal co-design would be beneficial.

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Author contributions

Y.Z., F.U. and H.W. conceived the concepts and perspectives in this article together and co-wrote the manuscript.

Competing interests

The authors declare no competing interests.

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